SAMSUNG SDI _ _

FOR MESSRS:

March 08. 2005

N.A.K.S

CUSTOMER SPECIFICATIONS

(COMMON USE COF/TCP TYPE).

1,269cm (50 Inch) Wide Plasma Display Module

MODEL : **S50HW-XB02**

M3 (S50HW-XD03)
(PAL/NTSC)

* This specification will be approved by both N.A.K.S and Samsung SDI Co.,Ltd.
* Please return one of this specification with your signature for approval.

Proposed by:

Signature Y.Y.Choo

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Samsung SDI Co., Ltd

Approved by:

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H-MDK-01

SAMSUNG SDI CO.,LTD.

Revision History

Revision	Date	Description Of Changes	Approval
1	March 08. 2005	Newly established	-

TABLE OF CONTENTS

1. DESCRIPTION

The S50HW-XD03 is a 50-inch wide full color plasma display Module with a resolution of 1366(H) × 768(V) pixels. The display module includes the Plasma Display Panel(PDP), the Panel driving electronics, the Logic Control Board, and the SMPS(PSU) . PSU consists of two pieces of board (main supply & image board supply).

2. FEATURES

- Wide aspect ratio(16:9) 50 inch diagonal display screen. The display area is 1106.46㎜ wide and 622.08㎜ high.
- Slim and light weight. The display Module is 60.1㎜ in depth and weight only approx.25.6㎏ exclusive of power supply.
- 134.2 million colors colors by combination of 9 bits R,G and B digital data
- High Luminance, High contrast, Wide viewing angle. The screen has a white peak Luminance of typical 1,000 cd/㎡(NTSC), contrast of typical 5,000:1(NTSC), contrast of Minimum 2,500:1(NTSC)
  and a viewing angle (of) greater than 160° comparable to those of CRTs.

3. PRODUCT NAME AND MODEL NUMBER

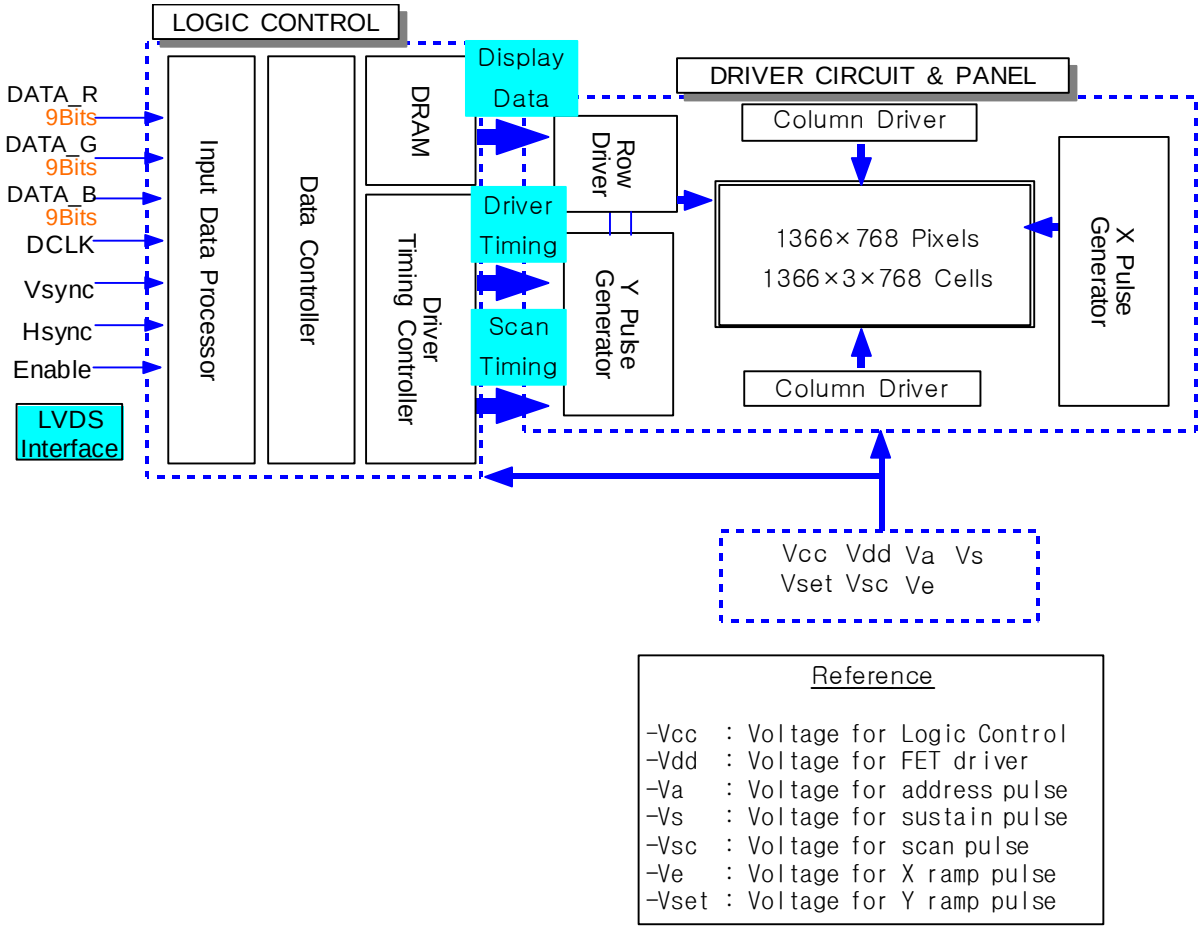
- Product name : 50 inch Full Color Plasma Display Module3
  (abbreviation : PDP Module3)
- Model number : S50HW-XD03

4. FUNCTION OUTLINE

- The plasma display Module has an APC(Automatic Power Control) function which restricts power consumption within the certain value with regard to each display load ratio.

- The plasma display Module is operated by following digital video signals; Vertical synchronous signal, Horizontal synchronous signal, Enable signal and 9bits data signal of each R,G, and B color. All signals are based on LVDS level.
- The plasma display Module is operated at 50Hz or 60Hz frame rate. An external frame rate conversion is required in order to display the other formats.
- The plasma display Module requires 8 types of input power voltages; voltage for LOGIC, voltage for COF driver IC, voltage for gate driver, voltage for sustain, erase, address, set and scan.
- The plasma display Module is operated at progressive signal only.
  An external progressive scan conversion is required in order to display the other formats.
- The plasma display Module requires rated 100~240V, 50~60Hz of input power voltage. Maximum input voltage rating is AC 90~264V.

5. BLOCK DIAGRAM



6. DISPLAY CHARACTERISTICS

6.1 Display Performance

No	Item	Rating		
1	Display Pixels	Horizontal 1366 × Vertical 768 pixels (1 pixel = 1 R,G,B cells)		
2	Display Cells	Horizontal 4,098 × Vertical 768 cells		
3	Pixel Pitch	Horizontal 810㎛ × Vertical 810㎛		
4	Cell Size	R	Horizontal 270㎛ × Vertical 810㎛	
		G	Horizontal 270㎛ × Vertical 810㎛	
		B	Horizontal 270㎛ × Vertical 810㎛	
5	Pixel Type	R, G, B Matrix (refer to Figure-2)		
6	Effective Display Size	Horizontal 1106.46㎜ × Vertical 622.08㎜		
7	Number of color	134.2 million colors		
8	Peak Luminance *1	typical 1,000cd/㎡ (NTSC)		
9	Contrast Ratio *2 (in dark room)	typical 5,000:1 (NTSC)	Calculated value Refer to note *2	
10	Color Coordinates (Typical value)	White : X= 0.285±0.020, Y= 0.290±0.020		
11	Viewing Angle *3	Over 160°		

(Note)

* 1. Luminance and Color Coordinates are the values that were measured with 1% load ratio white pattern. The condition for measurement is shown in Figure-3.
* 2. Contrast Ratio is calculated from the display Luminance and the non-display Luminance value. Display condition is shown in Figure-4.
* 3. Viewing angle is a critical angle at which the Luminance is reduced to 50% to the Luminance perpendicular to the PDP Module. The Luminance is measured by a contact luminance meter CA-100Plus.

6.2 Display Cell Arrangement

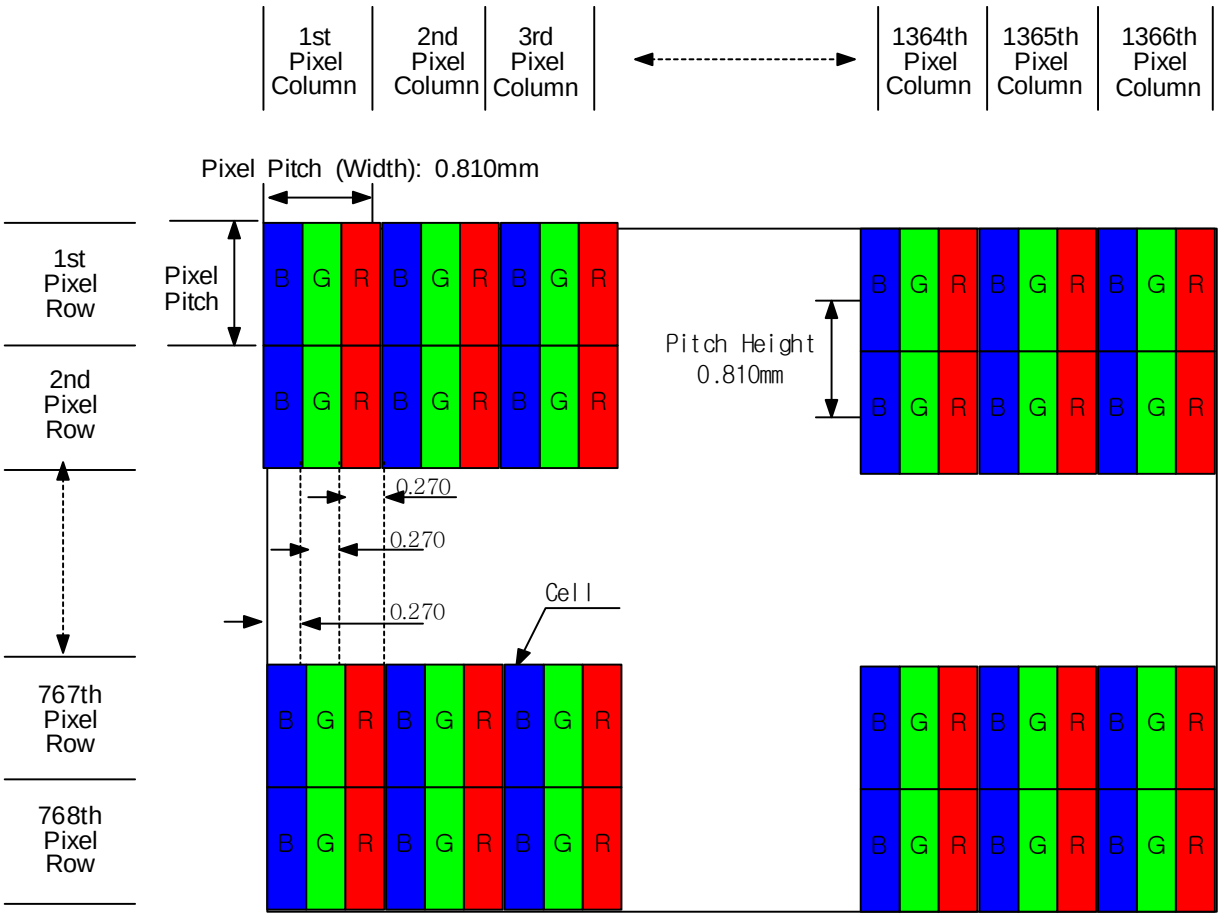


Figure-2. Display Cell Arrangement

6.3 Luminance Measurement Condition

(1) Display Pattern

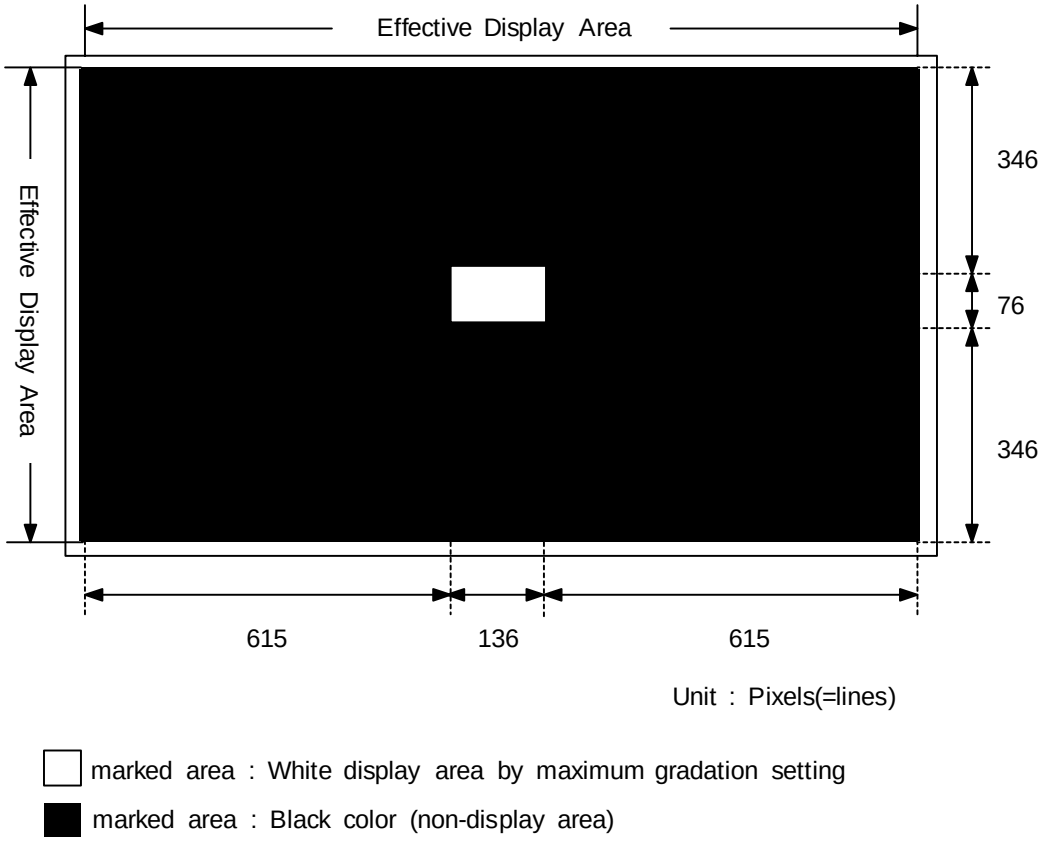


Figure-3. Display Pattern for Brightness & Contrast Ratio Measurement

(2) Display Area ratio : 1% white window

(3) Vsync : 16.7ms or 20ms

(4) Measuring equipment : MINOLTA CA-100Plus

(5) Ambient Temperature : Room Temperature

(6) Ambient Luminance : Dark Room (<2 lux)

6.4 Contrast Measurement Condition

(1) Measuring point

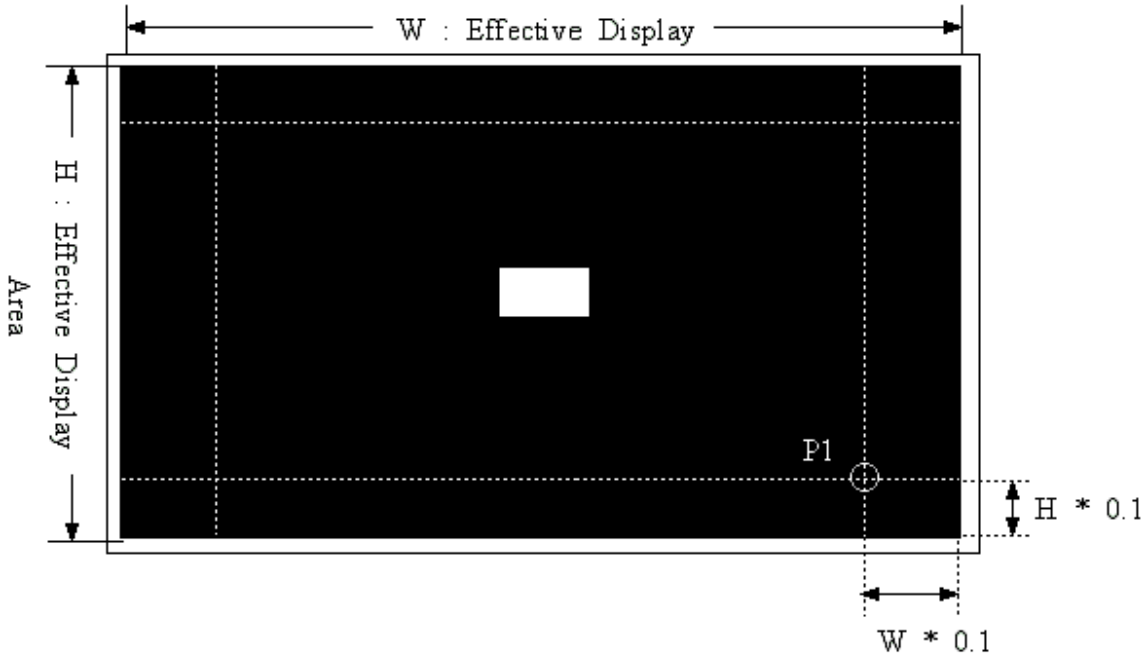


Figure-4. Measurement point

(2) Vsync : 16.7 ms or 20ms

(3) Measuring Equipment : MINOLTA CA-100Plus
Pattern Generator(VG-828, LVDS Output).

(4) Contrast Calculation formula

$$\text{Contrast ratio} = \frac{\text{Luminance of 1\% white window Area at the center of the screen}}{\text{Luminance of Black Area *1}}$$

【 Note 】

1. For mass production test purposes, it is recommended to measure just 1 point, P1 of Figure.-4 on display pattern of Fig.-3.

(5) Ambient Light : Dark Room (<2 lux)

6.5 Display Cell Defect Specification

In some cases, a panel may have defective cells that cannot be controlled.
These defective cells can be categorized into three types;
(1) Non-lighting cell defect : defect in which the cell is always off
(2) Non-extinguishing cell defect : defect in which the cell is always on.
(3) Flickering cell defect : defect in which the cell is flickering.
(4) High intensity cell defect : defect in which the cell is brighter than other cells
(5) Test Pattern : Full White, Full Red, Full Green and Full Blue with 511 gray level.

The display cell defect specifications define the allowed limits for display cell defects and are used as the criteria in determining whether a panel should be shipped.

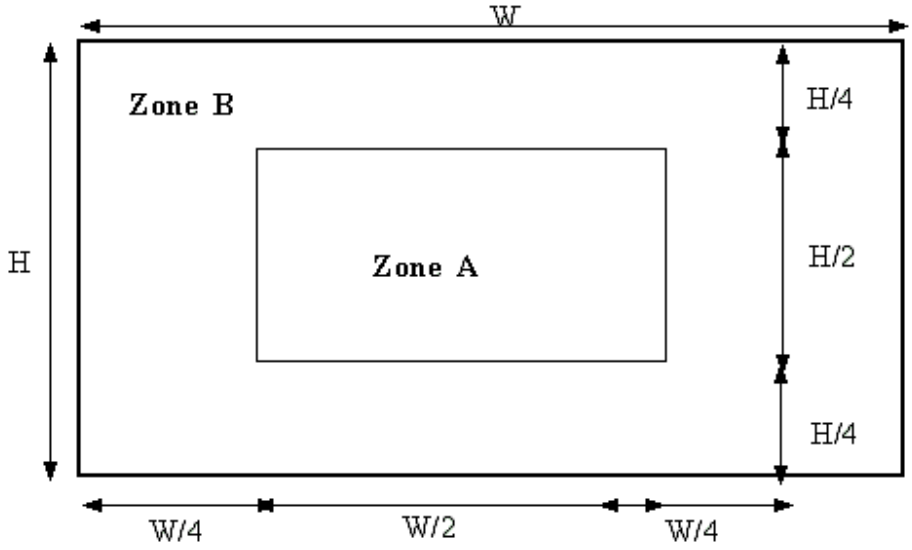


Figure-5. Measuring Area

Item	Specification	
	Number of cell defects	
Non-lighting cell defect	**Zone A: 4 and less**	**Zone B: 10 and less**
Non-extinguishing cell defect	**Zone A: 1 and less**	**Zone B: 3 and less**
Flickering cell defect	**Zone A: 1 and less**	**Zone B: 3 and less**
Continuous cell defect	**Zone A: 1 and less**	**Zone B: 1 and less**
Total defect	**Total number of cell defects** in **Zone A and B is less than 14**	

6.6 Luminance Variation Specification

The color-PDP uses ultraviolet light produced by gas discharge to illuminate phosphor. Uneven phosphor coating and inconsistent discharge characteristics cause slight difference in Luminance among the sections in a panel.

Item	Definition	Specification
Full white brightness variation	The brightness is measured at 9 points (A1~A9 of Fig-6) on full white pattern. The full white brightness variation as then calculated from the following equations.	10% and less
Equation	$\frac{Max - \bar{x}}{\bar{x}} \times 100\%$ & $\frac{\bar{x} - Min}{\bar{x}} \times 100\%$	

The Luminance variation specifications define the allowed limits for Luminance differences and are used as the criteria in determining whether a panel should be shipped.

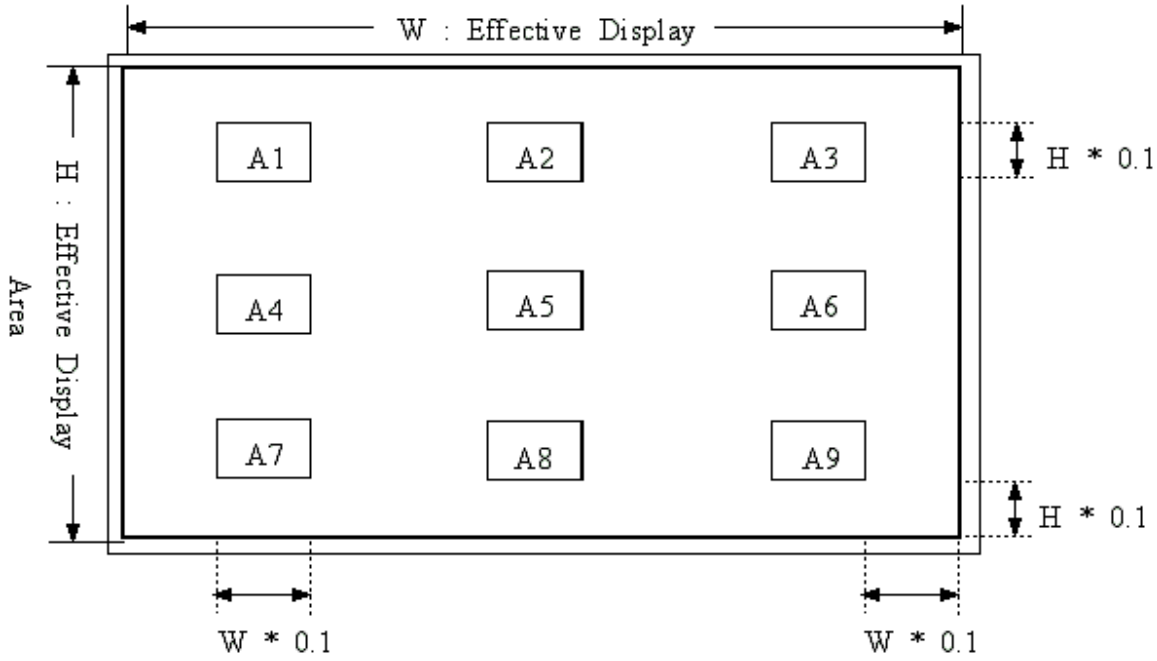


Figure-6. Measuring areas

6.7 Power consumption

(1) APC (Automatic Power Control) Function

The PDP has an APC (Automatic Power Control) function for the panel driver power source. If the total display load ratio exceeds approximately 11%, total power consumption will not exceed certain level. Measurement results below include gamma (=2.2) function.

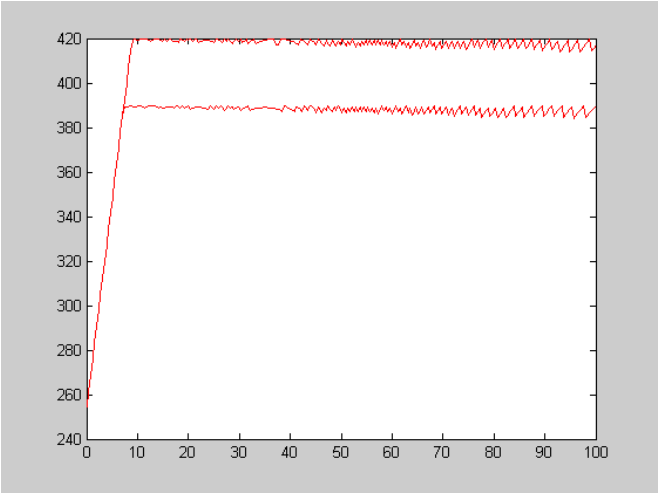


Figure-8. Display Load Ratio vs. power consumption

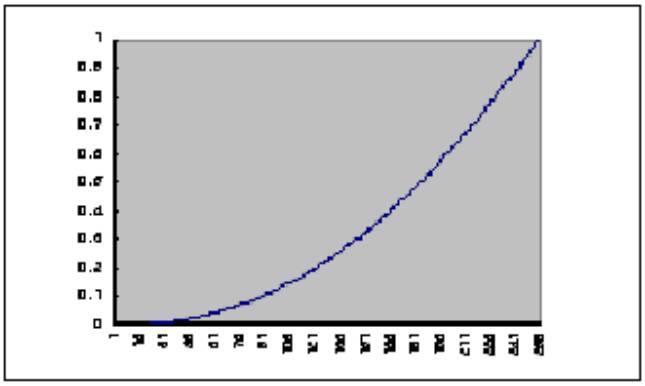
(2) Power consumption specification

Power consumption	Power sources
390 + 10%W and less	AC 120V, 220V 60Hz

【 Note 】

1. This is the case that the PDP Module includes SMPS.
2. It is measured on a full screen white pattern.

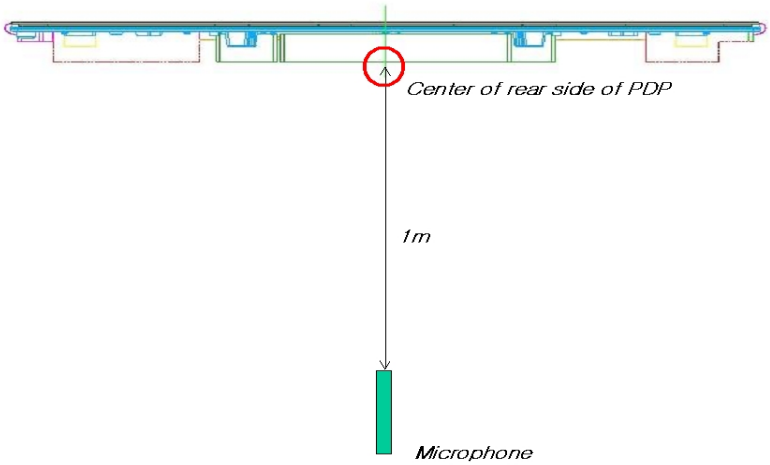
6.8 Gamma characteristics



7. SOUND PRESSURE LEVEL SPECIFICATION

7.1 Measurement Condition

(1) Background Noise Level : less than 18dBA
(2) Measuring Pattern : Dynamic Images **(only, Full Black to Full White)**
(3) Measuring Equipment : Sound level meter Type 2827 made by B&K
(4) Measuring Distance : 1m from the rear side of PDP Module
(5) Measuring point



7.2 Sound Pressure Level : **Typical 32 dB**

- Frequency Range : 50Hz ~ 8kHz
- Bandwidth : ⅓ Octave
- Weighting Filter : A-weighting network

【 Note 】

1. Sound Pressure Level is **the overall level** calculated from the individual band levels of 50Hz ~ 8kHz.
2. PSU must be included in this measurement.
3. The most noisy dynamic patterns are used in this measurement.

8. MECHANICAL CHARACTERISTICS

8.1 Mechanical Specifications

No	Item	Rating
1	Outer Dimensions	Width 1,184㎜ × Height 700㎜ × Thickness 63㎜ (mounting TCP) *see Appendix (Mechanical Dimensions Drawing)
2	Weight	Approx. 25.6 kg (exclusive of power supply)

* Appendix A1 is included in section 12.1
* Appendix A2 is included in section 12.2.

8.2 Mechanical Characteristics

No	Item	Rating
1	Vibration	Frequency : 10 to 55Hz Sweep rate : 1 octave/min Stroke : x,y direction : 0.35㎜ z-direction : 0.175㎜
2	Shock	Acceleration : less than 20G (X,Y-direction) less than 10G (Z-direction) Duration : 11 ms

***** Notes: (Test condition) Non-Packaging, Operational (only for Vibration)
* Test time of Vibration Test is 30 minutes every direction(x,y,z)
* The number of times for shock test is 6 times every direction(x,y,z).

9. ENVIRONMENTAL CONDITIONS

9.1 Absolute Maximum Ratings

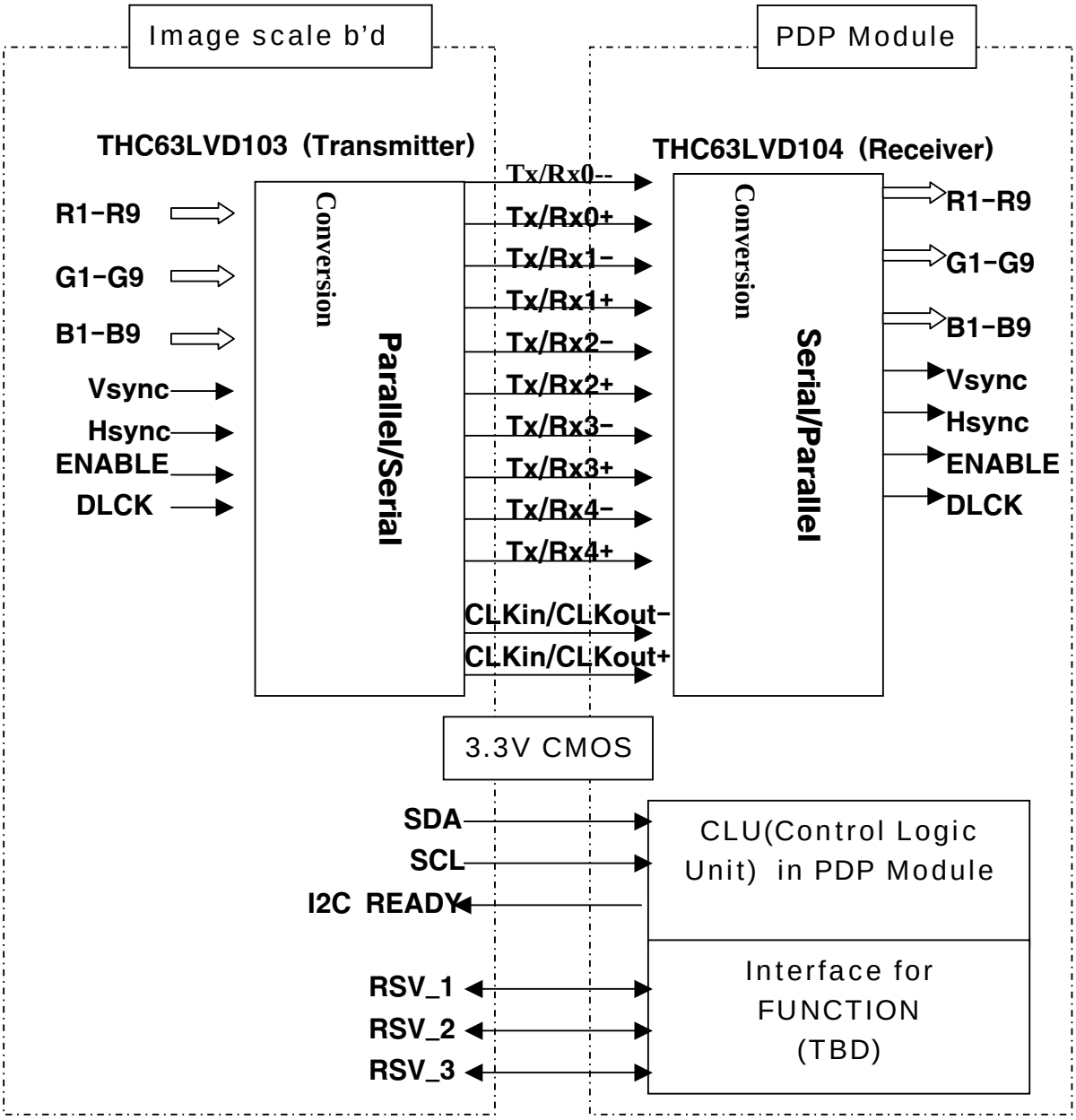
No.	Item	Rating	
1	Temperature	Operational	0 to 65℃
		Storage	-15 to 70℃
2	Humidity	Operational	5 to 85 % RH (no condensation)
		Storage	5 to 85 % RH (no condensation)
3	Pressure	Operational	700 to 1114 hPa (0~3,000m)
		Storage	300 to 1114 hPa (0~9,000m)

9.2 Recommended Environmental Condition

No.	Item	Rating	
1	Temperature	Operational	0 to 50℃
		Storage	-15 to 60℃
2	Humidity	Operational	20 to 70 % RH (no condensation)
		Storage	20 to 80 % RH (no condensation)
3	Pressure	Operational	800 to 1114 hPa (0~2,000m)
		Storage	600 to 1114 hPa (0~4,500m)

10. Interface Signal Specifications

10. 1. Configuration Context



10. 2. Interface Function Specifications (input data and display processing)

- 1366-dot data signals are inputted to this product to display data.
- The Video signal and control signal input section uses a low voltage differential signaling (LVDS) interface.
- An I2C bus serial data interface is used for the communication between MPU of FTV side and the CLU (Control LOGIC Module) of this PDP Module.
- I2C_READY signal is used that the CLU(Control LOGIC Unit) of PDP module inform image scale b'd that CLU is ready for I2C communication.(1 : ready, 0 : not ready)

10. 3. Input Signal Definition

No	Item	Signal name		Q	I/O	Method	Definition
1	Display Signal	Video Signal	RXIN0- RXIN0+ RXIN1- RXIN1+ RXIN2- RXIN2+ RXIN3- RXIN3+ RXIN4- RXIN4+	1 1 1 1 1 1 1 1 1 1	Input	LVDS Differentials	Differential serial data signal. Input video and timing signals after differential serial conversation using a dedicated transceiver. The serial data signal is transmitted seven times faster than the base signal.
		Dot Clock	RXCLKIN- RXCLKIN+	1 1	Input	LVDS Differential	Differential clock signal. Input the clock signal after differential conversation using a dedicated transceiver. The clock signal is transmitted at the same speed as the base signal.
2	MPU Communication	Communication	SDA SCL I2C_READY	1 1 1	Input	LVTTL (I2C)	I2C bus serial data communication signal. Communication with the CLU (Control Logic Module) of this product is enabled.

10. 4. LVDS Signal Definition and Function

A video signal (display data signal and control signal) is converted from parallel data to serial data with the LVDS transmitter and further converted into four sets of differential signals before inputted to this PDP Module. These signals are transmitted seven times faster than the dot clock signals. The dot clock signal is converted into one set of differential signals.
The LVDS signal definitions and functions are as follows (in Italic)::

Interface Signal Function			
Symbol	I/O	Function	Remarks
RxIN0-	I	Display Data Signal: R2, R3, R4, R5, R6, R7, G2	LVDS signal
RxIN0+	I		LVDS signal
RxIN1-	I	Display Data Signal: G3, G4, G5, G6, G7, B2, B3	LVDS signal
RxIN1+	I		LVDS signal
RxIN2-	I	Display Data Signal: B4, B5, B6, B7, Hsync, Vsync, DE	LVDS signal
RxIN2+	I		LVDS signal
RxIN3-	I	Display Data Signal and Control Signal: R8, R9, G8, G9, B8, B9	LVDS signal
RxIN3+	I		LVDS signal
RxIN4-	I	Display Data Signal R1, G2, B1	LVDS signal
RxIN4+	I		LVDS signal
RxCLKIN-	I	Dot Clock Signal: CLK	LVDS signal
RxCLKIN+	I		LVDS signal
SDA	I	I2C serial data	3.3V CMOS
SCL	I	Clock signal for SDA	3.3V CMOS
I2C_READY	O	I2C enable signal	3.3V CMOS

10. 5. Video Signal Definition and Function

The table below indicates the definitions and functions of input video signals before LVDS conversion.

Interfaces Signal Functions		
Symbol	**Function**	**Remarks**
R9 to R1	9 bits red video signal (note 1)	Display data signal: R9: MSB*, R1: LSB**
G9 to G1	9 bits green video signal (note 1)	Display data signal: G9: MSB*, G1: LSB**
B9 to B1	9 bits blue video signal (note 1)	Display data signal: B9: MSB*, B1: LSB**
Hsync	Horizontal synchronous signal	This signal specifies the data period for one horizontal line. Control of the next line begins at the rising edge of Hsync.
Vsync	Vertical synchronous signal	Timing signal that controls the start of the screen. Control of the next screen begins at the rising edge of Vsync.
DCLK	Clock for video signal	Latch the video signal at falling edge.

* MSB: Most Significant Bit (Highest Intensity Bit)
**LSB: Least Significant Bit (Lowest Intensity Bit)
Note 1: The RGB signal may be compensated with Inverse γ circuit (E/D (=Error Diffusion) must be included) before inputted to the PDP Module. In order to obtain good characteristic of low level's gray scale, inverse γ correction and E/D process are advisory to be performed after inputted to the PDP Module.

10.6. Electrical Condition of Interface Signal

10.6. 1. Maximum Ratings

Common conditions : Ta = 25℃, Vcc = 3.3V

Absolute Ratings						
Item			**Parameter**	**Symbol**	**Ratings**	**Module**
Input Signals	LVDS	Rx0-/+,Rx1-/+,Rx2-/+, Rx3-/+, Rx4/+,CLKin-/+	Input Voltage	Vi	-0.3~3.6	V
	3.3V CMOS	SDA, SCL RSV1/2/3(TBD)	Input Voltage	Vi	-0.3~3.6	V

10. 6. 2. Electrical Characteristics

Common conditions : Ta = 0℃ ~ +70℃, Vcc = 3.0V ~ 3.6V

Electrical Characteristics							
Signal	**Item**	**Symbol**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Module**
LVDS	High level input voltage	V_{th}	V_{CM}=1.2V	-	-	100	mV
	Low level input voltage	V_{tl}	V_{CM}=1.2V	-100	-	-	mV
	Input current	I_{in}	V_{IN} = +2.4V/0V Vcc = 3.6V	-	-	±20.0	μA
I2C	Input Voltage	V_{ih}		0.5*Vcc	-	4.1	V
		V_{il}		-0.5	-	0.3*Vcc	V
	Input Capacitance	V_{in}	-	-	-	8	pF
	Output Voltage	V_{oh}	I_{oh} = 8 mA	2.4	-	-	V
		V_{ol}	-	-	-	0.4	V
	Output Current	I_{ol}	-	-	-	10	mA
3.3V CMOS	High level input voltage	V_{ih}	-	2.0	-	-	V
	Low level input voltage	V_{il}	-	GND	-	0.8	V
	Input current	I_i	V_I=Vcc or GND	-	-	±10.0	μA
	High level output voltage	V_{oh}	Io = -1 mA	2.4	-	-	V
	Low level output current	V_{ol}	I_o = 1 mA	-	-	0.4	V

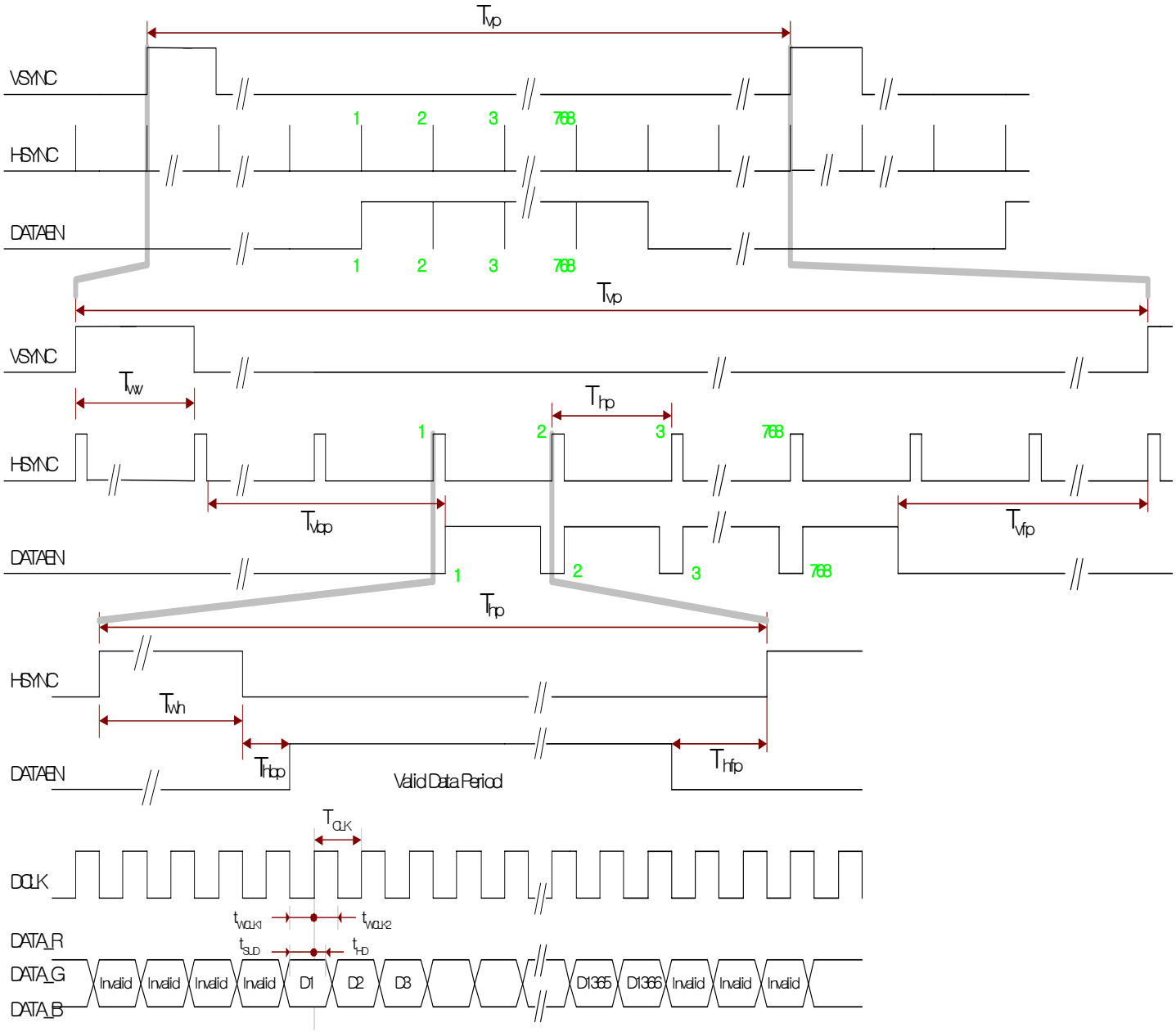
10. 7. Video Signal Interface Timing Conditions

The table below indicates the conditions of input video signal before LVDS conversion. These conditions must be satisfied. Refer to the figure of the timing chart.

60Hz(NTSC)					
ITEM	Symbol		Typ	Unit	Note
DCLK	Period	Tclk	13.51	ns	
	Frequency		74	MHz	
Hsync	Period	Thp	1504	Tclk	
	Period		20.32	us	
	Frequency	Fh	49.20	KHz	
	Width	Twh	22	Tclk	
Vsync	Period	Tvp	820	Thp	
	Frequency	Fv	60	Hz	
	Width	Twv	6	Thp	
DE (Data Enable)	Horizontal Valid	Thv	1366	clk	
	Horizontal Back Porch	Thbp	50	clk	
	Horizontal Front Porch	Thfp	66	clk	
	Horizontal Blank		138	Thp-Thv	
	Vertical Valid	Tvv	768	H	
	Vertical Back Porch	Tvbp	10	H	
	Vertical Front Porch	Tvfp	36	H	
	Vertical Blank		52	Tvp-Tvv	

50Hz(PAL)					
ITEM	Symbol		Typ	Unit	Note
DCLK	Period	Tclk	13.51	ns	
	Frequency		74	MHz	
Hsync	Period	Thp	1504	Tclk	
	Period		20.32	us	
	Frequency	Fh	49.20	KHz	
	Width	Twh	22	Tclk	
Vsync	Period	Tvp	984	Thp	
	Frequency	Fv	50	Hz	
	Width	Twv	6	Thp	
DE (Data Enable)	Horizontal Valid	Thv	1366	clk	
	Horizontal Back Porch	Thbp	50	clk	
	Horizontal Front Porch	Thfp	66	clk	
	Horizontal Blank		138	Thp-Thv	
	Vertical Valid	Tvv	768	H	
	Vertical Back Porch	Tvbp	10	H	
	Vertical Front Porch	Tvfp	200	H	
	Vertical Blank		216	Tvp-Tvv	

Video Input Signal Timing Chart



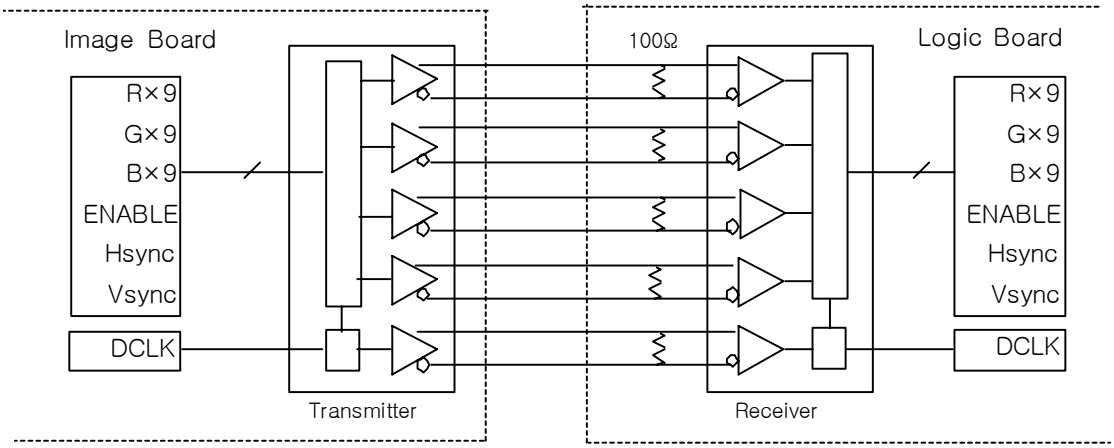
10. 8. LVDS Interface Timing Conditions

This PDP Module uses an LVDS interface for the signal input. For details of the input signal timing conditions, refer to the data sheets prepared by the LVDS transmitter IC maker. This PDP Module uses National Semiconductor's THC63LVD104..

10. 9. LVDS Connection Specifications

The following Figure shows the connection specifications and signal assignments of the LVDS interface IC. Do not connect or disconnect the connector when the system power in on. Otherwise, the LVDS interface IC could be damaged.

LVDS Interface Connection



LVDS Transmitter Pin Assignment

	Tx SIGNAL (THC63LVD103, Thine)					Rx SIGNAL (THC63LVD104) ,Thine					
	SCALER BOARD LVDS			Tx_Connector		Rx_Connector		LOGIC BOARD LVDS			
	PIN No	PIN NAME	SIGNAL	PIN No	PIN Name	PIN No	PIN Name	PIN No	PIN NAME	SIGNAL	
INPUT	12	CLK IN	Dot Clock	1	N.C.	1	N.C.	31	CLK OUT	Dot Clock	OUTPUT
	33	TA0	R(2)	2	GND	2	GND	47	RA0	R(2)	
	34	TA1	R(3)	3	SDA	3	SDA	46	RA1	R(3)	
	35	TA2	R(4)	4	GND	4	GND	45	RA2	R(4)	
	36	TA3	R(5)	5	SCL	5	SCL	43	RA3	R(5)	
	37	TA4	R(6)	6	GND	6	GND	42	RA4	R(6)	
	38	TA5	R(7)	7	EMGY_OUT	7	EMGY_OUT	41	RA5	R(7)	
	40	TA6	G(2)	8	TxOUT4+	8	RxIN4+	40	RA6	G(2)	
	41	TB0	G(3)	9	TxOUT4-	9	RxIN4-	39	RB0	G(3)	
	42	TB1	G(4)	10	I2C_READY	10	I2C_READY	38	RB1	G(4)	
	44	TB2	G(5)	11	GND	11	GND	36	RB2	G(5)	
	45	TB3	G(6)	12	TxOUT3+	12	RxIN3+	35	RB3	G(6)	
	46	TB4	G(7)	13	TxOUT3-	13	RxIN3-	34	RB4	G(7)	
	48	TB5	B(2)	14	GND	14	GND	33	RB5	B(2)	
	49	TB6	B(3)	15	GND	15	GND	32	RB6	B(3)	
	50	TC0	B(4)	16	TxCLKOUT+	16	RxCLKIN+	29	RC0	B(4)	
	52	TC1	B(5)	17	TxCLKOUT-	17	RxCLKIN-	28	RC1	B(5)	
	53	TC2	B(6)	18	GND	18	GND	27	RC2	B(6)	
	54	TC3	B(7)	19	GND	19	GND	26	RC3	B(7)	
	55	TC4	HSYNC	20	TxOUT2+	20	RxIN2+	25	RC4	HSYNC	
	57	TC5	VSYNC	21	TxOUT2-	21	RxIN2-	24	RC5	VSYNC	
	58	TC6	EN	22	GND	22	GND	22	RC6	EN	
	59	TD0	R(8)	23	GND	23	GND	21	RD0	R(8)	
	61	TD1	R(9)	24	TxOUT1+	24	RxIN1+	20	RD1	R(9)	
	62	TD2	G(8)	25	TxOUT1-	25	RxIN1-	19	RD2	G(8)	
	63	TD3	G(9)	26	GND	26	GND	18	RD3	G(9)	
	64	TD4	B(8)	27	GND	27	GND	17	RD4	B(8)	
	1	TD5	B(9)	28	TxOUT0+	28	RxIN0+	15	RD5	B(9)	
	3	TD6	-	29	TxOUT0-	29	RxIN0-	14	RD6	-	
	4	TE0	R(0)	30	GND	30	GND	13	RE0	R(0)	
	5	TE1	R(1)	31	GND	31	GND	12	RE1	R(1)	
	6	TE2	G(0)	R0, G0, B0 => GND				11	RE2	G(0)	
	8	TE3	G(1)					10	RE3	G(1)	
	9	TE4	B(0)					8	RE4	B(0)	
	11	TE5	B(1)					7	RE5	B(1)	
	16	TE6	N.C.					6	RE6	N.C.	
OUTPUT	23	TCLK-	Dot Clock	TCLK- => TxCLKOUT-		RxCLKIN- => RCLK-		56	RCLK-	Dot Clock	INPUT
	22	TCLK+		TCLK+ => TxCLKOUT+		RxCLKIN+ => RCLK+		57	RCLK+		
	31	TA-	R2~R7, G2	TA- => TxOUT0-		RxIN0- => RA-		49	RA-	R2~R7, G2	
	30	TA+		TA+ => TxOUT0+		RxIN0+ => RA+		50	RA+		
	29	TB-	G3~G7, B2, B3	TB- => TxOUT1-		RxIN1- => RB-		51	RB-	G3~G7, B2, B3	
	28	TB+		TB+ => TxOUT1+		RxIN1+ => RB+		52	RB+		
	25	TC-	B4~B7, HSYNC,VSYNC,DE	TC- => TxOUT2-		RxIN2- => RC-		54	RC-	B4~B7, HSYNC,VSYNC,DE	
	24	TC+		TC+ => TxOUT2+		RxIN2+ => RC+		55	RC+		
	21	TD-	R8,R9,G8,G9,B8, B9	TD- => TxOUT3-		RxIN3- => RD-		59	RD-	R8,R9,G8,G9,B8, B9	
	20	TD+		TD+ => TxOUT3+		RxIN3+ => RD+		60	RD+		
	19	TE-	R0,R1,G0,G1,B0, B1	TE- => TxOUT4-		RxIN4- => RE-		61	RE-	R0,R1,G0,G1,B0, B1	
	18	TE+		TE+ => TxOUT4+		RxIN4+ => RE+		62	RE+		

10. 10. I2C Interface Conditions

10. 10. 1. Basic Specifications

This PDP Module has the I2C bus serial data communication function.
The customer may use this function to make settings for PDP Module characteristics of several items.

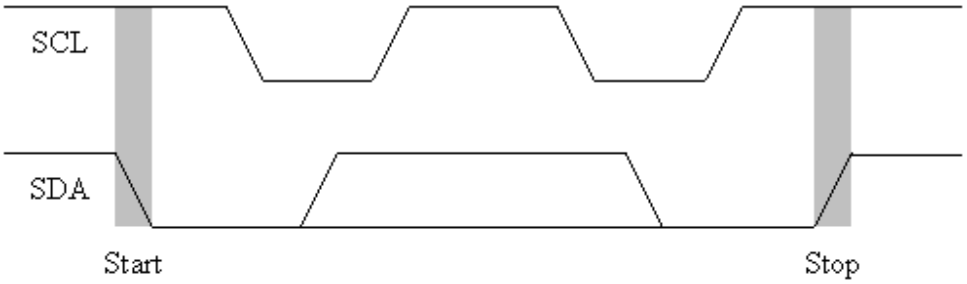
No	Parameter	Specifications
1	Transfer Rate	100 kbps
2	Device Status	Slave Receiver
3	Slave Address	CC(Write), CD(Read)

10. 10. 2. Data Validity

Amount of data that is transferred is 1-Bit per 1 SCL cycle. Data is valid when SCL is high and recognized as to state of SDA.

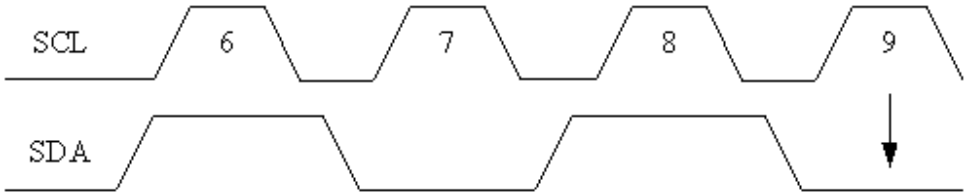
10. 10. 3. Start & Stop Condition

Start /Stop condition is generated by Master (=Image B'D). Before start condition or after stop condition, a SDA cannot be recognized as valid data.
Start condition ☞ SCL high & SDA transition from H to L
Stop condition ☞ SCL high & SDA transition from L to H



10. 10. 4. Acknowledge

When Master (=Image B'D) needs to stop reading data, the master should give NO ACK signal to salve by SDA. Slave (=PDP Module) gives ACK whenever 8-bit transfer is done.



10. 10. 5. 7-Bit Addressing for Device address(with example of CC or CD)

Master could choose slave by 7-bit slave address and decide what procedure is by R/W bit (H=Read procedure, L=Write procedure).

1	**1**	**0**	**0**	**1**	**1**	**0**	R/W	ACK

10. 10. 6. 16-Bit Mode

The basic I2C format (8-bit (Byte)) is expanded by 16-bit (Word). Therefore this PDP Module's I2C architecture consists of 7-bit slave addressing, 16-bit base addressing and 16-bit data (Refer to 'Write & Read Operation').

10. 10. 7. Data Transfer Sequence (Write)

The basic I2C format (8-bit (Byte)) is expanded by 16-bit (Word). Therefore this PDP Module's I2C architecture consists of 7-bit slave addressing, 16-bit base addressing and 16-bit data (Refer to 'Write & Read Operation').
Note 1: Black letters mean master (=Image B'D)'s bus occupation.
Note 2: Blue letters mean slave (=PDP Module)'s bus occupation.

START	Slave Address	W	ACK				
Base Address (Upper Byte)			ACK	Base Address (Lower Byte)		ACK	
Receive Data (Upper Byte)			ACK	Receive Data (Lower Byte)		ACK	
Receive Data (Upper Byte) [2N]			ACK	Receive Data (Lower Byte) [2N + 1]		ACK	STOP

10.10. 8. Data Transfer Sequence (Read)

The basic I2C format (8-bit (Byte)) is expanded by 16-bit (Word). Therefore this PDP Module's I2C architecture consists of 7-bit slave addressing, 16-bit base addressing and 16-bit data (Refer to 'Write & Read Operation').

Note 1: In advance, master should initialize writing sequence by giving base address and stop condition.

Note 2: After start condition and slave addressing, master could receive data from slave.

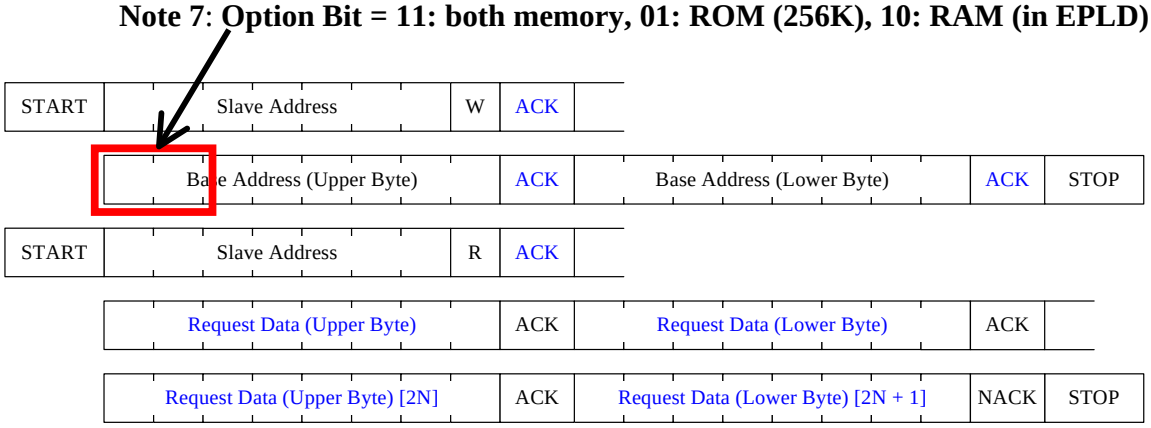
Note 3: Master should give acknowledge whenever 8-bit data is received.

Note 4: 'No acknowledge' could make master give stop condition on bus. Therefore, NACK is used for master to stop receiving data from slave.

Note 5: Black letters mean master (=Image B'D)'s bus occupation.

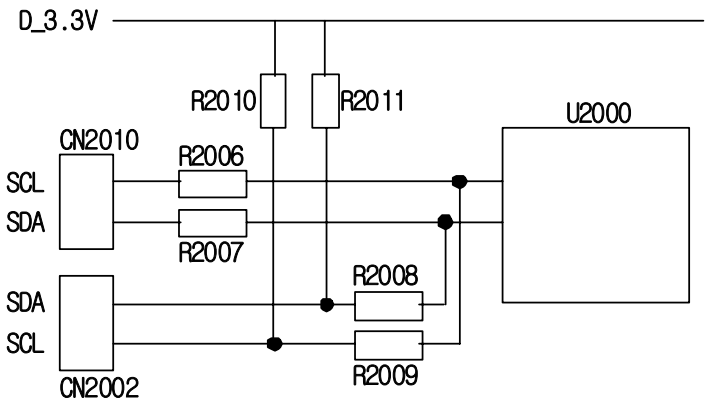
Note 6: Blue letters mean slave (=PDP Module)'s bus occupation.

Note 7: **Option Bit = 11: both memory, 01: ROM (256K), 10: RAM (in EPLD)**



10. 10. 9. Interface Circuit

(1) This PDP Module uses EPLD EP20K400EBC652-1 of ALTERA. For the electric characteristics, refer to the data sheet that is issued by ALTERA Co.ltd.

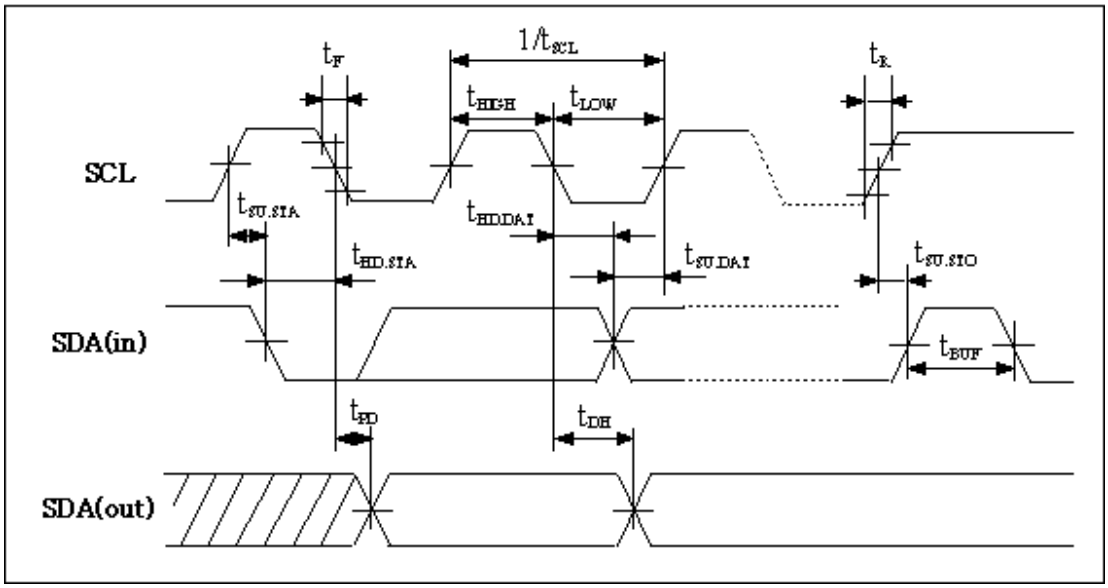


* 33 KOhm : R2010,R2011
* 220 Ohm : R2006,R2007,R2008,R2009
* CN2002 : Internal control port
* CN2010 : Port for Image board

10. 10. 10. I2C Bus Timing Specifications

* Refer to the following data merely as sample data.

No	Item	Symbol	Standard			
			Min.	Typ.	Max.	Module
1	SCL Input Frequency	f_{SCL}	-	50	200	㎑
2	SCL Input “HIGH” Period	t_{HIGH}	0.3	-	-	㎲
3	SCL Input “Low” Period	t_{LOW}	0.5	-	-	㎲
4	Start Condition Set Up Time	$t_{SU.STA}$	0.3	-	-	㎲
5	Start Condition Hold Time	$t_{HD.STA}$	0.3	-	-	㎲
6	Data Input Set Up Time	$t_{SU.DAT}$	0.1	-	-	㎲
7	Data Input Hold Time	$t_{HD.DAT}$	0	-	-	㎲
8	Stop Condition Set Up Time	$t_{SU.STO}$	0.3	-	-	㎲
9	Data Output Delay Time	t_{PD}	0.1	-	-	㎲
10	Data Output Hold Time	t_{DH}	0.1	-	-	㎲
11	SDA Bus Free Time	t_{BUF}	0.5	-	-	㎲
12	SCL, SDA Input Rising Time	t_R	-	-	0.8	㎲
13	SCL, SDA Input Falling Time	t_F	-	-	0.3	㎲
14	SCL, SDA Line Capacitor	C_b	-	-	400	㎊



10. 10. 11. Address Map

The address map is shown below. It could be changed in the next version. Always refer to 'address Map Version'. There are two regions of address map and one is for NTSC and the other is for PAL. Sub address that is shown below is for NTSC. Sub address region for PAL is 2000h~3FFFh. Basically address map for PAL is the same as NTSC's beside sub address. For example, 0080h for NTSC is correspondent to 2080h for PAL. Specially region of 0000h~007Fh is used commonly for NTSC & PAL.

* Slave Address ☞ Write: 66 (hex), Read: 66 (hex)

Sub Address	**Data**																**Note**
AF~0	**DF**	**DE**	**DD**	**DC**	**DB**	**DA**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
0001															NP		R/W
0078	Display Version in Hex(=00)								Display Size in Hex (42"=2A)								R
0079	256K Version in Hex(=00)								FPGA Version in Hex(=00)								R
0080			Pattern Select														R/W
0081								Data Level									R/W
009C								DF									R/W
00C4				APC_Data Hold Time													R/W
00DE								IE									R/W
20DE								IE									R/W

Note 1. The region except the table that is shown above is system area.
Customers are not recommended to control or write data on system without any notice to SDI..

Note 2. 0001~007F : common area for NTSC & PAL.
0080~1FFF : Area for NTSC system.
2080~3FFF : Area for PAL system.

Details of Settings

Sub Address	Data Bit	Symbol	Item / Function	Setting [hex]		Note
				Range	Initial	
0001	0~1	NP	NTSC/PAL Select (valid only when internal pattern is activated)	10 / 01	10	*(a)
0080 2080	8~D	PS	Pattern Select ☞ Patterns below are valid when **IE** (Internal clk or External clk) is set to '1'. 00: Full Window (Black) 01~04: Full Window (White, Red, Green, Blue) 05~08: 9 Point Box (White, Red, Green, Blue) 09: 4% Window , 0A: Color Bar 0B~0E: Cross Bar (White, Red, Green, Blue) 0F: Cross Hatch 10: Dot Array 11: 50% Gray 12~13: Gray Bar (Vertical, Horizontal) 14~15: Vertical Ramp Pattern (Stay, Scroll) 16~17: Horizontal Ramp Pattern (〃)	00~17	01	*(a)
0081 2081	0~8	DL	Data Level ☞ Patterns below are valid when **IE** (Internal clk or External clk) is set to '1'. 01~FF: 0~255 Gray Level.	00~1FF	1FF	*(a)
009C 209C	8	DF	**Diffusion Filter Enable** (1=ON, 0=OFF) * Initial value : 00(NTSC), 00(PAL)	0 or 1	0(NT) 0(PA)	*(c)
00C4 20C4	8~F	APC_DHT	**APC Level Shift Speed** (00=0sec, 0A=0.167sec) * Initial value : 0A(NTSC), 0C(PAL))	00~0A	0A	*(b)
00DE 20DE	8	IE	**Internal Pattern Enable** (1=ON, 0=OFF) ☞ If you set 00DE and 20DE all to '1', you can drive internal pattern with external CLK for both NTSC and PAL by switching '0001' as '10' or '01'.	0 or 1	0	*(a)

*(a): Please access these address for test use only.
For ordinary operating conditions, values if these address should be set to initial values.
*(b): Customers can set these values considering their specifications.
*(c): Diffusion Filter – This filter disperses dynamic false contour at continuous gray level of input data(for example, human body). SDI Module uses same number of SF(11) for NTSC and SF(14) for PAL. By using this option, dynamic false contours of SDI Module in PAL

could be decreased a little.

10. 11. Connector Specifications

Rx_Connector	
PIN No	PIN Name
1	N.C.
2	GND
3	SDA
4	GND
5	SCL
6	GND
7	EMGY_OUT
8	RxIN4+
9	RxIN4−
10	I2C_READY
11	GND
12	RxIN3+
13	RxIN3−
14	GND
15	GND
16	RxCLKIN+
17	RxCLKIN−
18	GND
19	GND
20	RxIN2+
21	RxIN2−
22	GND
23	GND
24	RxIN1+
25	RxIN1−
26	GND
27	GND
28	RxIN0+
29	RxIN0−
30	GND
31	GND

1.CN2010 connector is located in Logic Board.

2. Pin to Pin pitch of connector CN2010 is 0.625mm.

3. The length of mating cable to CN2010 is recommended to be not longer than 25.0cm.

4. Pin numbering order : Right to Left view from component side of Logic Board.

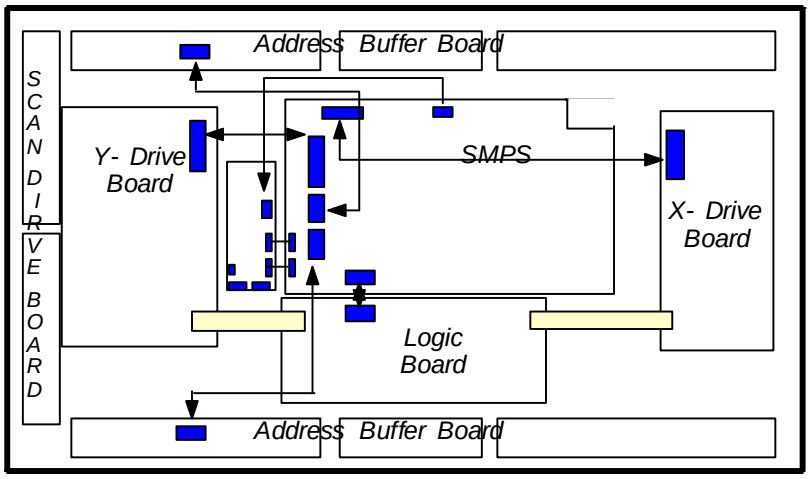
5. Reserved for factory use only. This pin should be disconnected in case of customer's use.

[Note]

1 : If using a long cable, applied voltage may be dropped because of its resistance. Specified voltage should be applied correctly at the input of the module side connector.

11. SMPS SPECIFICATIONS

11.1 Connector Location



[Note]

1. Layout Schematic is viewed from back side of PDP Module.
2. The Output Power for Image board is separated from Main SMPS.
3. The Power for Image board is output by DC link Voltage boosted through PFC.
4. The Input Power Connector in Y-Drive Board is named as "SY".
5. The Input Power Connector in X-Drive Board is named as "SX".
6. The Input Power Connector in Logic Board is named as "SL".
7. The Input Power Connector in Address Buffer Board is named as "BUFFER"..

11.2 Power Specification

Power Name	Voltage(V)	Current(A)	Regulation(%)	Ripple & Noise (Vpp,mV)	Remarks
Vs	170	3.0	±5	1000	Sustain voltage
Va	70	2.5		500	Address voltage
15Vg	15	1.5		100	Drive gate in FET
D5VL	5	3.0		50	Drive TTL in X,Y driving, Logic
D3V3	3.3	3.0		50	Drive IC in Logic
5Vsb	5.1~5.15	2.0		50	

[Note]

1. Above voltage levels are norminal value. They are adjustable to drive Panel.

11.3 Detail Power Specification of SMPS

11.3.1 DC outputs for Logic Board

Connector No.	Output Name	Nominal Voltage	Load Current(A)			Variable Range(V)	Remarks
			Min.	Max.	Peak.		
CN8008	D3V3	3.3V	0.2	-	3.0	2.8~3.8	
	D5VL	5V	-	-	2.0	4.5~5.5	
	Vs_on	3.0V	-	-	-	-	Active High
CN8006 CN8005	Va	70V	0.2	1.2	2.5	60~75	

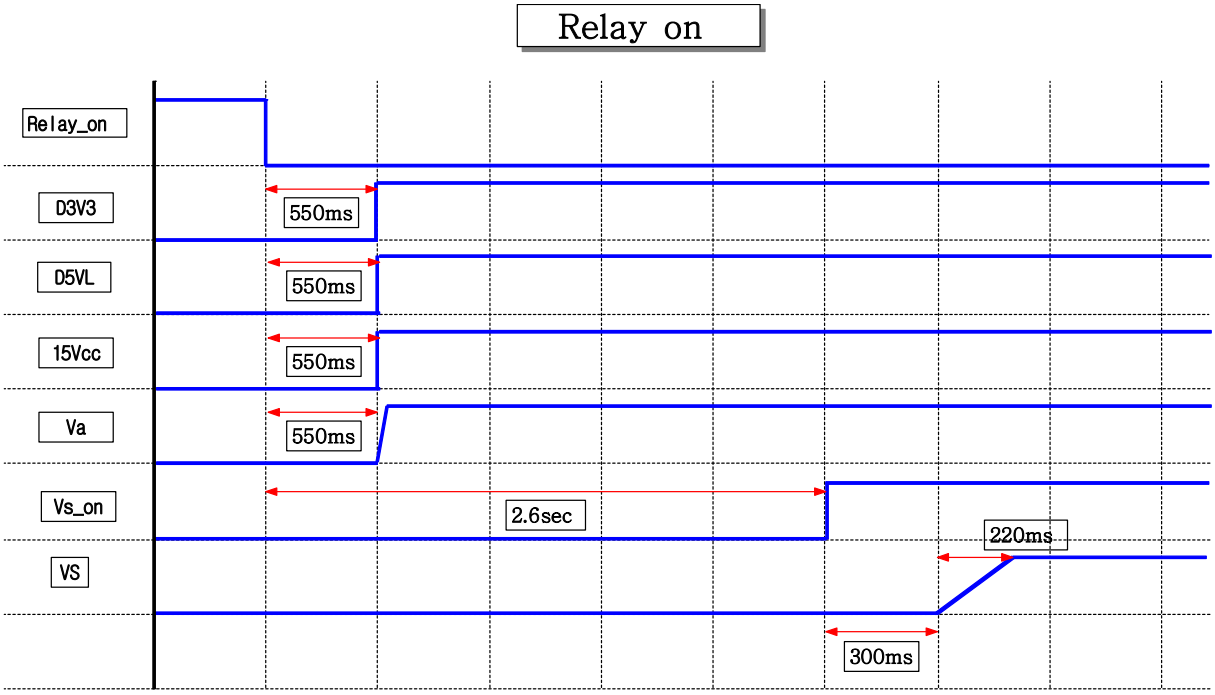
11.3.2. DC outputs for Driving Board(X,Y)

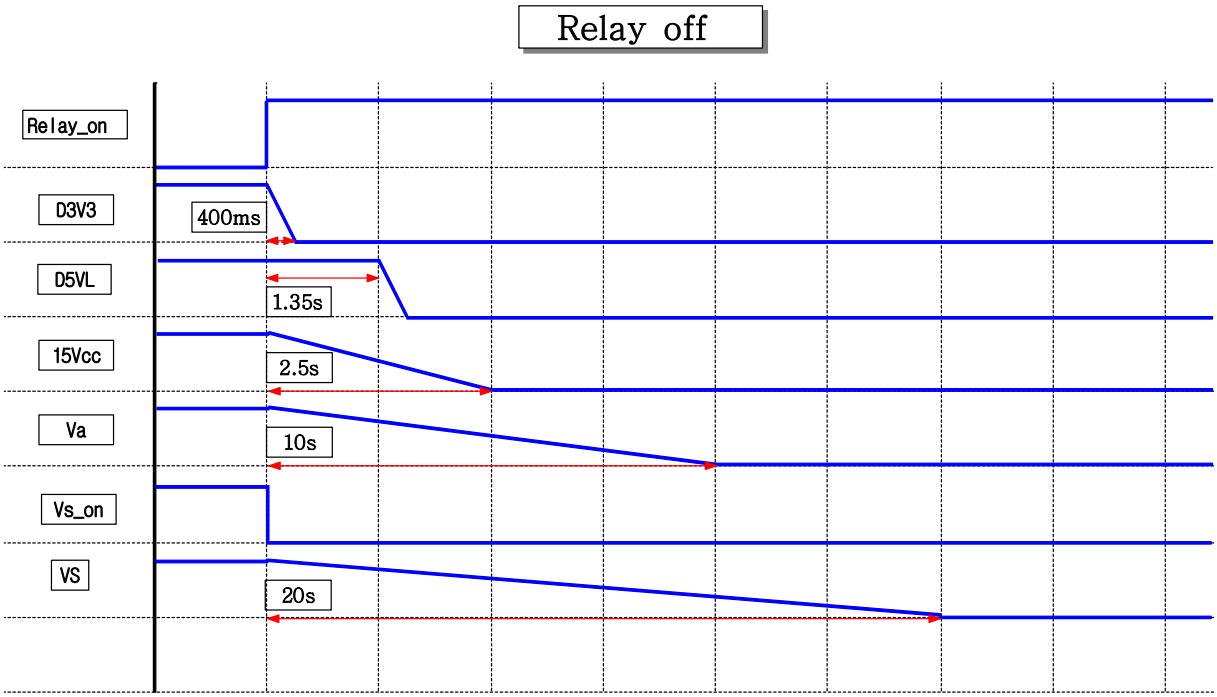
Connector No.	Output Name	Nominal Voltage	Load Current(A)			Variable Range(V)	Remarks
			Min.	Max.	Peak.		
CN8002 CN8003	D5VL	5V	0.2	-	1.0	4.5~5.5	
CN8002 CN8003	15Vg	15V	0.1	1.0	1.5	14~16	
CN8002 CN8003	Vs	170V	0.1	2.5	3.0	160~180	

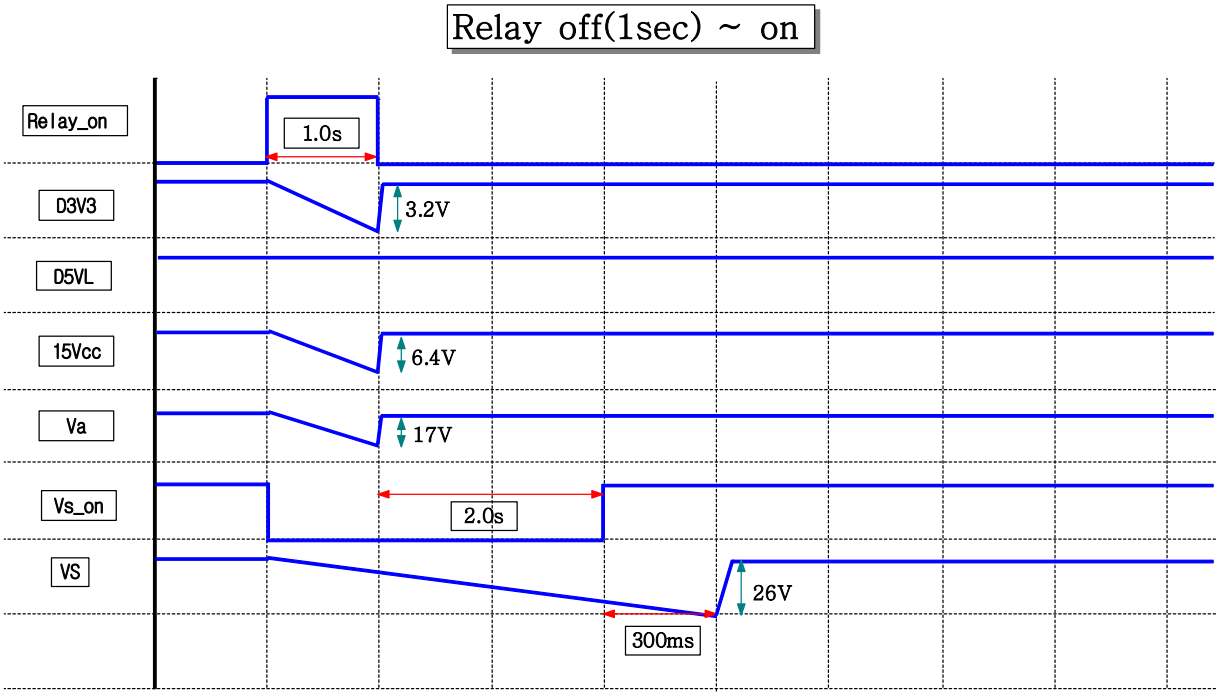
11.3.3 DC outputs for Image Scaler Board

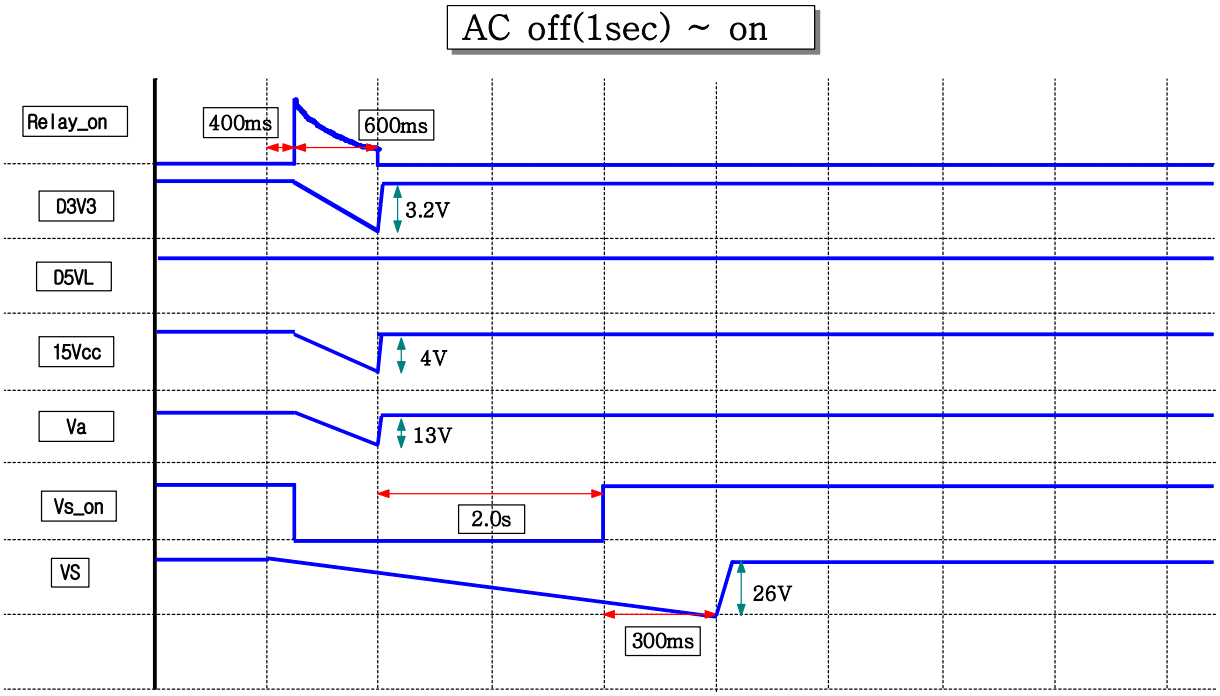
Connector No.	Output Name	Nominal Voltage	Load Current(A)			Remarks
			Min.	Max.	Peak.	
CN9003	VT	33V	0	-	0.01	
CN9003	12Vamp	12V	0.3		2.5	
CN9004	D12V	12V	0.1		0.6	
CN9003	A12V	12V				
CN9004	D6V	6V	0.1		1.0	
CN9003	A6V	6V	0.1		1.0	
CN9004	D3V3	3.3V	0.1		1.5	

11.4 Power Applying Sequence






Relay off(1sec) ~ on
Relay_on
1.0s
D3V3
3.2V
D5VL
15Vcc
6.4V
Va
17V
Vs_on
2.0s
VS
26V
300ms


AC off(1sec) ~ on
Relay_on
400ms
600ms
D3V3
3.2V
D5VL
15Vcc
4V
Va
13V
Vs_on
2.0s
VS
26V
300ms

11.5 Pin assignment of connectors for Power Supply

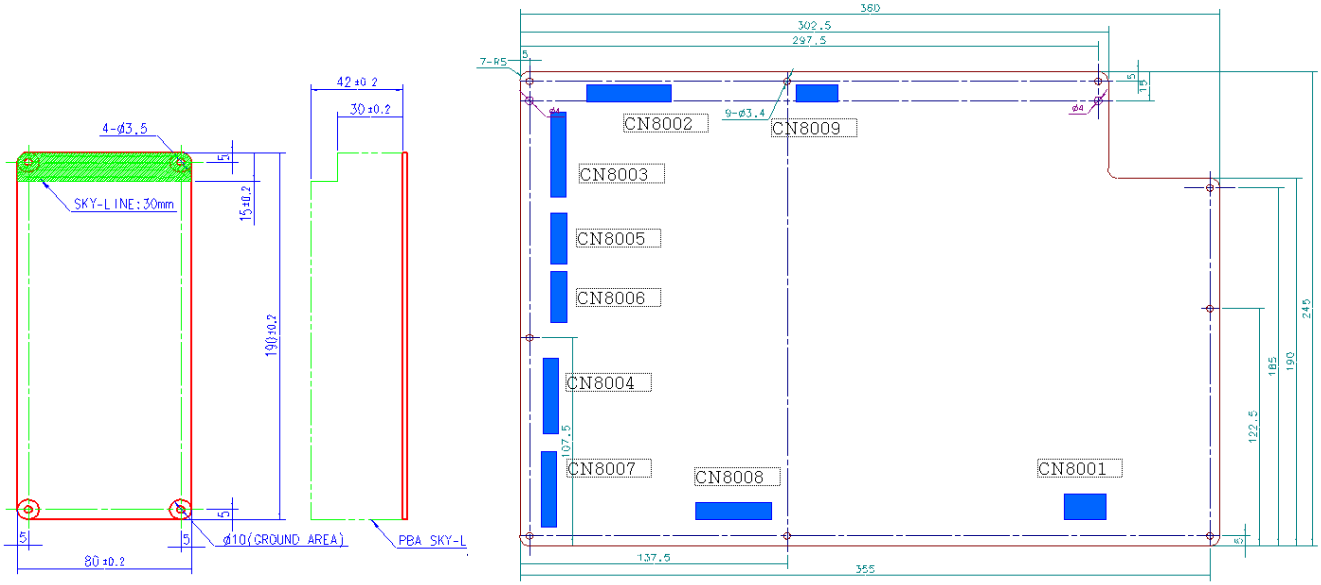
11.5.1 Power MAIN BOARD Output Connector & Pin Assignment

Location Num.	CN8001	CN8002	CN8003	CN8004	CN8005 CN8006	CN8007	CN8008	CN8009
Function	AC Input	X Drive	Y Drive	Interface	Address Buffer	Interface	Logic	DC_LINK
Pin Num.	3 Pin	9 Pin	10 Pin	13 Pin	5 Pin	12 Pin	10 Pin	5 Pin
Connector Type	JST B2P3-VH	Molex 35313-0910	Molex 35313-1010	Molex 35312-1310	Molex 35313-0510	Molex 35312-1210	Molex 5267-1010	Molex 35313-0510
Pin No.	Pin Name	Pin Name	Pin Name	Pin Name	Pin Name	Pin Name	Pin Name	Pin Name
1	AC Line	D5VL	D5VL	Relay	Va	VSB	D3V3	PFC
2	N.C	Vg	Vg	Panel_Power	Va	GND	D3V3	N.C
3	AC Netural	GND	GND	GND	N.C	THEM.DET	GND	0V
4		GND	NC	N.C	GND	GND	GND	0V
5		NC	GND	IV-4	GND	NC	D5V	DC-Vcc
6		GND	NC	GND		GND	GND	
7		GND	GND	IV-3		GND	VSB	
8		Vs	GND	GND		PIRQ	Relay	
9		Vs	Vs	IV-2		N.C	Vs_on	
10			Vs	GND		N.C	GND	
11				IV-1		N.C		
12				GND		N.C		
13				NC				

11.5.2 IMAGE BOARD Output Connector & Pin Assignment

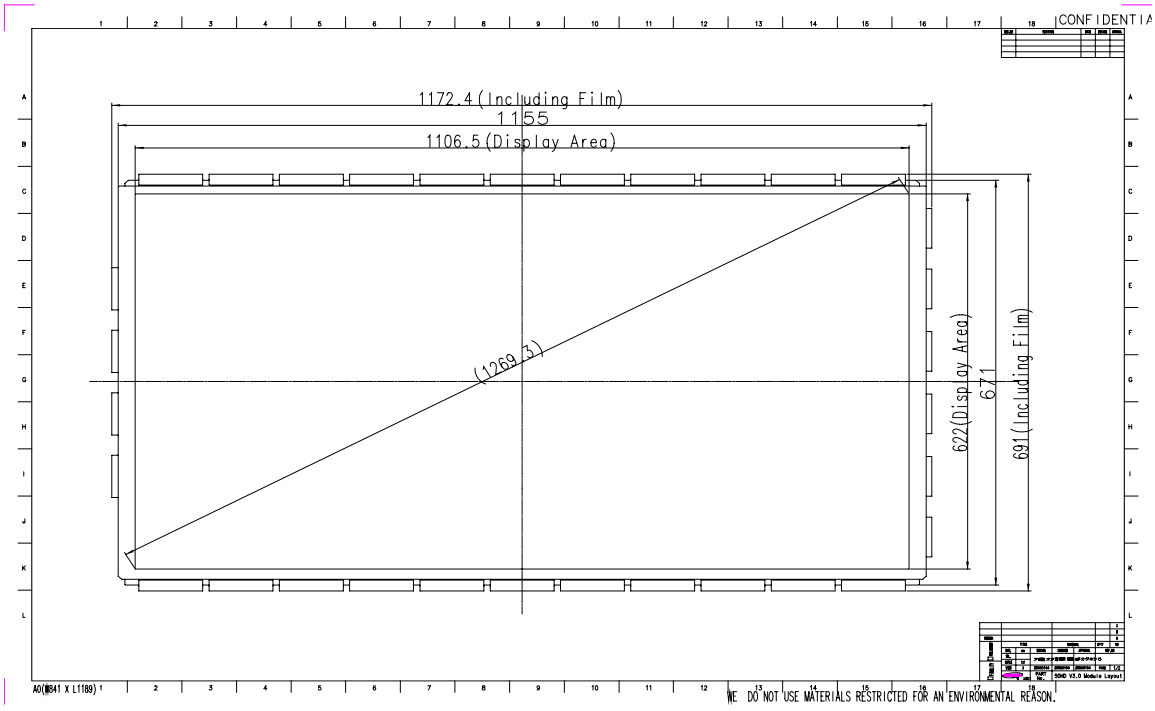
Location Num.	CN9002	CN9003	CN9004	CN9005	CN9006	CN9007
Function	FAN	-	-	DC-LINK	Interface	Interface
Pin Num.	3 Pin	10 Pin	11 Pin	5 Pin	12 Pin	13 Pin
Connector Type	Molex 35312-0310	Molex 35313-1010	Molex 35313-1110	Molex 35312-0510	Molex 35313-1210	Molex 35313-1310
Pin No.	Pin Name	Pin Name	Pin Name	Pin Name	Pin Name	Pin Name
1	FAN12V	A6V	D6V	PFC	VSB	Relay
2	GND	GND	GND	NC	GND	Panel power
3	NC	A12V	D3V3	0V	THEM.DET	GND
4		GND	D3V3	0V	GND	NC
5		VAMP	GND	DC_VCC	NC	IV-4
6		VAMP	GND		GND	GND
7		GND	D12V		GND	IV-3
8		GND	Relay		PIRQ	GND
9		VT	GND		N.C	IV-2
10		GND	VSB		N.C	GND
11			Them.det		N.C	IV-1
12					N.C	GND
13						N.C

11.6 MECHANICAL REQUIREMENTS



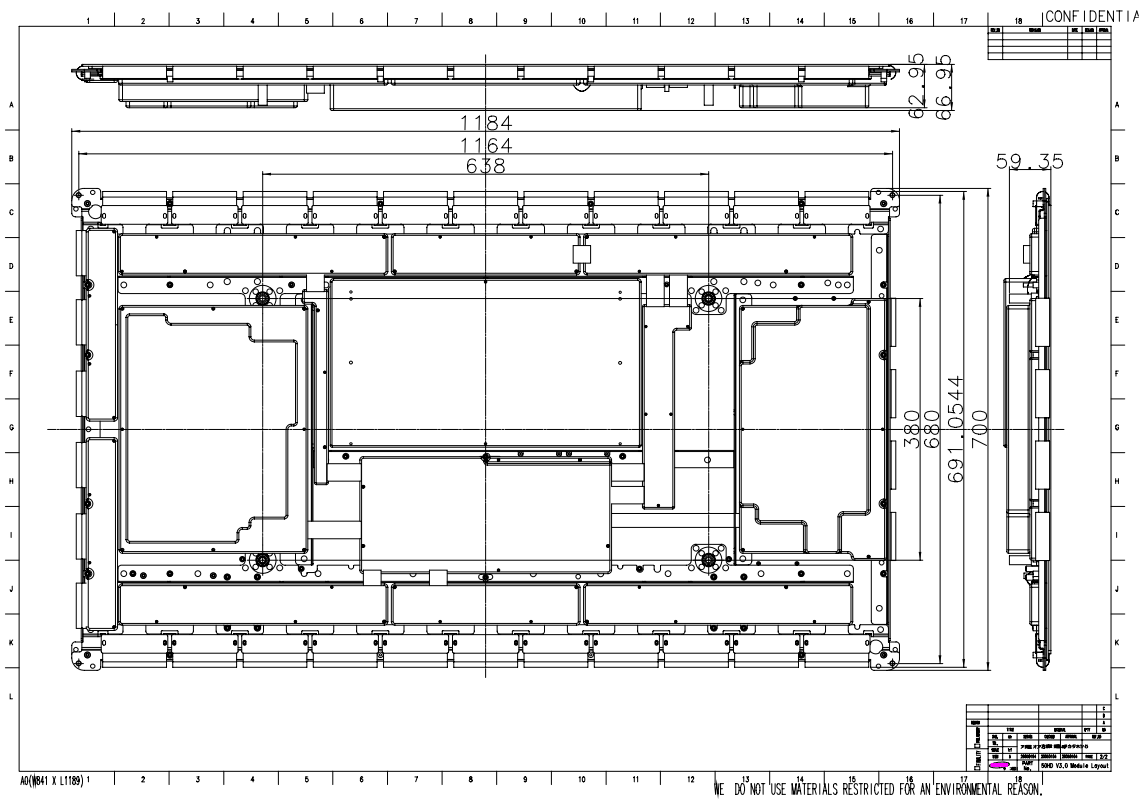
12. Mechanical Dimension Drawing

12.1. Front Side



Appendix A1

12.2. Rear Side



Appendix A2

13. Label

13.1 Label Type

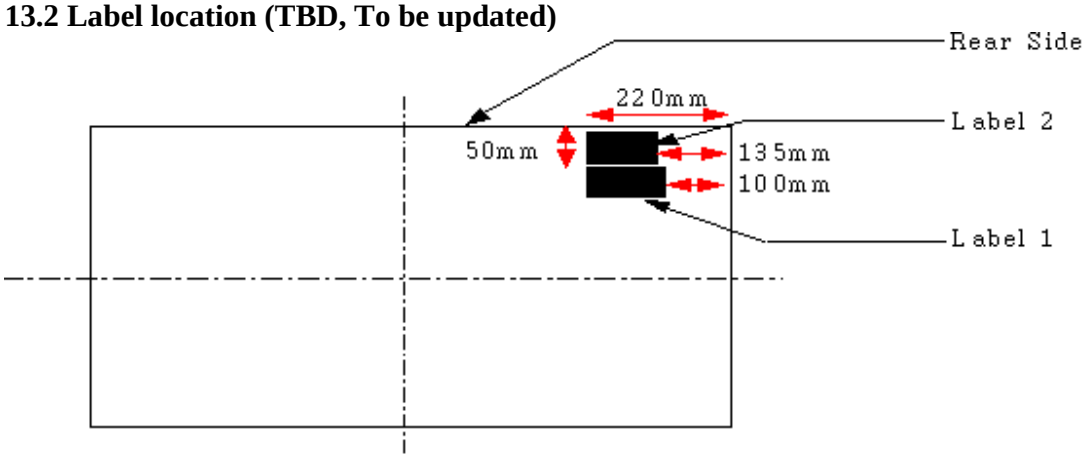
(1) Label for the PDP Module

(To be included)

(2) Label for power specification

(To be included)

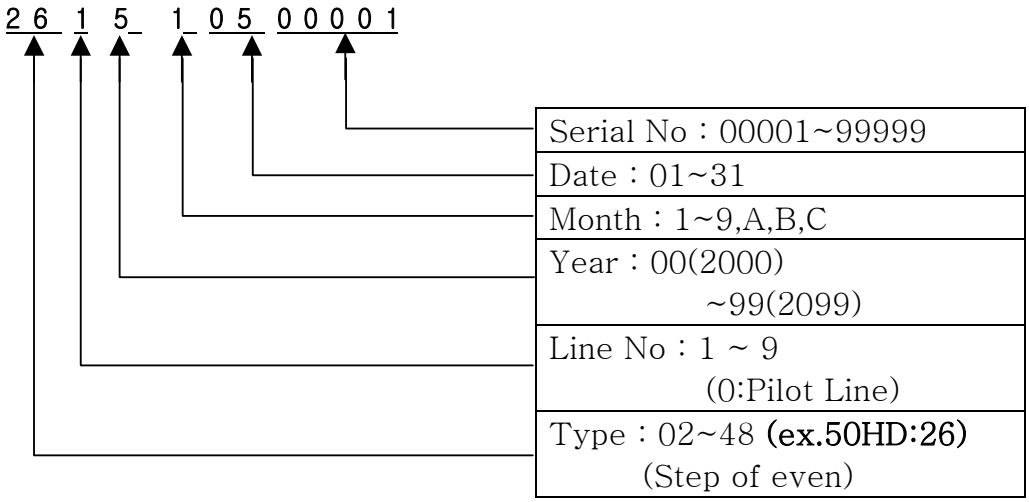
13.2 Label location (TBD, To be updated)



【 Notes 】

1. Label-1 is a label for the PDP Module.
2. Label-2 is a label for the power specification.

13.3 Serial No.



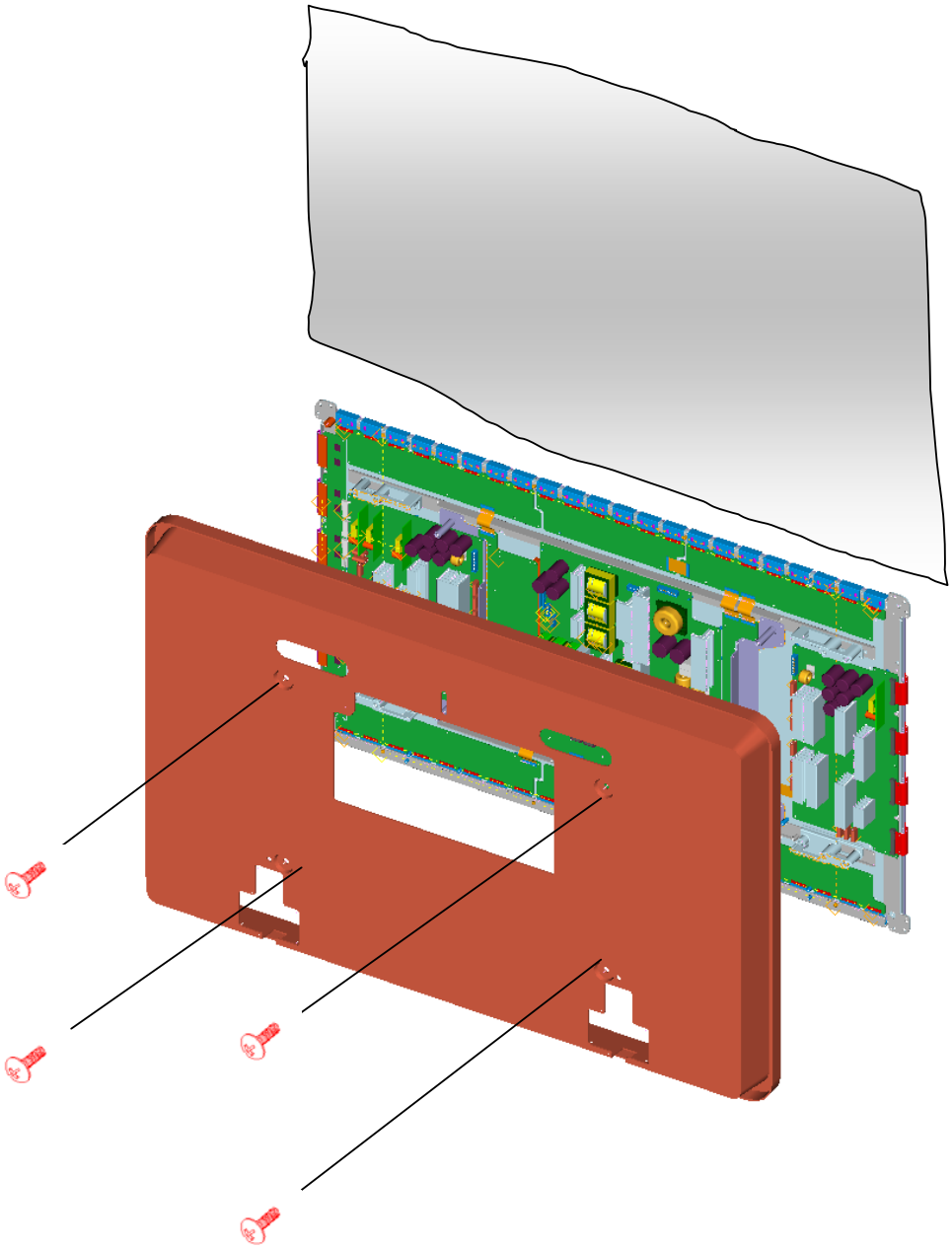
14. Packing

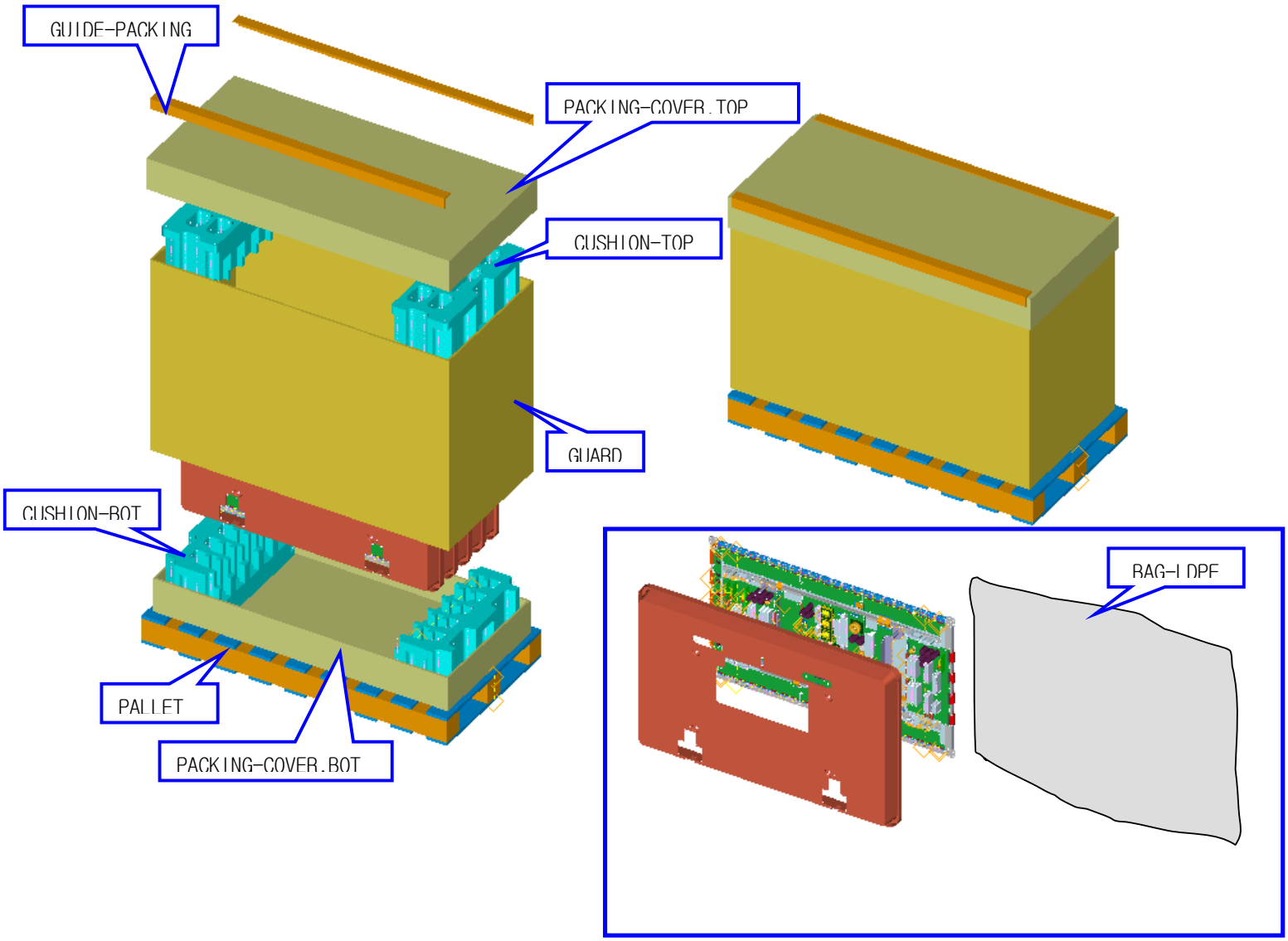
14.1 Packing Dimension and Parts List

- **Number of Module in 1 package: 5 Modules**
- **Packing dimensions (W*L*H): 1465*760*1106 (mm) (Including Pallet :136mm)**
- **Weight: About 140 ± 5 (Kg)**

No.	Parts	Specification	Q'ty	Remarks
1	Bag LDPE	W1300,L950,T0.07	1,000	(Unit: Module1 **1000 pcs**)
2	Silicagel(DRY-PAK)	100g	2,000	
3	Cover-Module(P/W10)	L1251,W791,H79.3	200	
4	Washer	IDØ8.5,ODØ35,2T	4,000	
5	Screw,Machine	PH,+,M8,L25	4,000	
6	Pallet	L1465,W760,H136	200	
7	Packing-Cover-Top	L1477,W722,H155	200	
8	Packing-Cover-Bot	L1417.W662,H165	200	
9	Cushion,Bottom	50HD,EPP,V3,TCP,C=0.022	400	
10	Cushion-Top	50HD,EPP,V3,TCP,C=0.022	400	
11	Band,PE	T1,W18mm	800M	
12	Band,Clip,Locker	SPL,18mm,T0.35	800	
13	Guide,Pack	L1465,D50,T5	400	
	Module 2			

14.2 **Packing Assay drawing**




GUIDE-PACKING
PACKING-COVER.TOP
CUSHION-TOP
GUARD
CUSHION-BOT
PALLET
PACKING-COVER.BOT
BAG-LDPE

15. RELIABLITY

15.1 Expected Service Life

#1. Definition

The expected service life is defined by the following two categories.
And the life time is defined by either (1) or (2), whichever occurs first.

(1) The white color Luminance level becomes half (50%) of its initial value, which is determined by the phosphor characteristics.

(2) The number of display cell defects increases to double the specification value, which is depending on the discharge characteristics.

#2. Test condition and life time

The expected service life time varies depending on the display conditions set forth below.

(1) Full screen white color display

Life time : 60,000 hours

* Test condition : 8Hr/Day

16. WARNING / CAUTION / NOTICE

TO PREVENT POSSIBLE DANGER, DAMAGE, AND BODILY HARM, PLEASE CONSIDER AND OBSERVE ALL WARNINGS AND CAUTIONS CONTAINED IN THIS PARAGRAPH.

16.1 Warning

If you do not consider the following warnings, it could result in death or serious injury

(1) The S50HW-XD03 Module is controlled by high voltage about 350V. If you need to handle the Module during operation or just after power-off, you must take proper precautions against electric shock and must not touch the drive circuit portion and metallic part of S50HW-XD03 Module within 5 minutes.
The capacitors in the drive circuit portion remain temporarily charged even after the power is turned off. After turning off the power, you must be sure to wait at least one minute before touching the Module. If the remain voltage is strong enough, it could result in electric shock.

(2) Do not use any other power supply voltage other than the voltage specified in this product specifications. If you use power voltage deviated from the specifications, it could result in product failure.

(3) Do not operate or install under the deviated surroundings from the environmental specification set for the below; in moisture, rain or near water-for example, bath tub, laundry tub, kitchen sink; in a wet basement; or near a swimming pool; and also near fire or heater - for example, near or over radiator or heat resistor; or where it is exposed to direct sunlight; or somewhere like that. If you use the S50HW-XD03 Module in places mentioned above, it could result in electric shock, fire hazard or product failure.

(4) If any foreign objects (e.g. water, liquid and metallic chip or dust) entered the S50HW-XD03 Module, the power supply voltage to the S50HW-XD03 Module must be turned off immediately. Also, never push objects of any kind into the S50HW-XD03 Module as they may touch dangerous voltage point or make short circuits that could result in fire hazard or electric shock.

(5) If smoke, offensive smell or unusual noise should come from the S50HW-XD03 Module, the power supply voltage to the S50HW-XD03 Module must be turned off immediately. Also, when the S50HW-XD03 screen fails to display any picture after the power-on or during operation, the power supply must be turned off immediately. Do not continue to operate the S50HW-XD03 Module under these conditions.

(6) Do not disconnect or connect the S50HW-XD03 Module's connector while the power supply is on, or immediately after power off. Because the S50HW-XD03 Module is operated by high voltage, and the capacitors in drive circuit remain temporarily charged even after the power is turned off. If you need to disconnect or reconnect it, you have to wait at least one minute after power off.

(7) Do not disconnect or connect the power connector by a wet hand. The voltage of the product may be strong enough to cause an electric shock.

(8) Do not damage the power cable of the S50HW-XD03 Module, also do not modify it.

(9) When the power cable or connector is damaged or frayed, do not use it.

(10) When the power connector is covered with dust, please wipe it out with a dry cloth before the power on.

16.2 Caution

If you do not consider the following cautions, it may result in personal injury or damage facilities.

(1) Do not set the S50HW-XD03 Module on an unstable place, vibrating place and inclined place. The S50HW-XD03 Module may fall or collapse, and it may cause serious injury to a person, and serious damage to the product.

(2) If you need to remove the S50HW-XD03 Module to another place, you must turn off the power supply and detach the interface cable and power cable from the S50HW-XD03 Module beforehand, and watch your steps not to step on the cables during the operation. If the cables are damaged during the transport, it may result in fire hazard or electric shock. Also if the S50HW-XD03 Module is dropped or fallen, it may cause a serious injury to a person.

(3) When you draw or insert the S50HW-XD03's cable, you must turn off the power supply and do it (with) holding the connector. If you forcibly draw the cable, the electric wire in the cable can be exposed or broken. It may result in fire hazard or electric shock.

(4) When you carry the S50HW-XD03 Module, it should be done with at least two workers in order to avoid any unexpected accidents.

(5) The S50HW-XD03 Module has a glass-plate. If the S50HW-XD03 Module is inflicted with excessive stress - for example; shock, vibration, bending or heat-shock, the glass plate could be broken. It may result in a personal injury. Also, do not press or strike the glass surface.

(6) If the glass panel was broken, do not touch it with bare hand. It may result in a cut injury.

(7) Do not place any object on the glass panel. It may be the cause of the scratch or break of the glass panel.

(8) Do not place any object on the S50HW-XD03 Module. It may result in a personal injury due to fall or drop.

16.3 Notice

When you apply the S50HW-XD03 Module to your system or handle it, you must make sure to follow the notices set forth below.

□ Notice to your system design

(1) The S50HW-XD03 Module radiates the infrared rays of between 800 and 1000㎚. It may bring an error in operating the IR-remote controller or another electric system. Please consider (to) providing the IR absorb filter in your system, and evaluating it.

(2) The S50HW-XD03 Module has a high-voltage switching circuit and a high-speed clock circuit. Therefore, you have to apply and evaluate the EMC consideration of your system.

(3) The S50HW-XD03 Module has a glass plate. In your mechanical design, please (consider to) avoid any excessive shock and stress to the glass surface. Also be careful not to demage the tip-tube at the corner of glass plate. If the glass plate and tip-tube are damaged, the S50HW-XD03 Module may fail.

(4) In your system, for your safety, please have the remaining voltage of the S50HW-XD03 Module leaked immediately after power-off.

(5) As the S50HW-XD03Module generates heat during operation, please make sure the well-radiation and well-ventilation are provided for your system design. The S50HW-XD03 Module may be defected by the usage out of the specified ambient temperature.

(6) The ventilation design in your system should have a back-cover that is able to prevent moisture and dust from getting into the inside of the electric circuit, because the S50HW-XD03 Module has high-density electric parts with high-voltage. If the driver circuit has condensation or dusts, it may cause a short circuit or dielectric breakdown.

(7) If the S50HW-XD03 Module displays a fixed pattern on the screen for are extended period of time, it could make the differences in Luminance and chromaticity between fixed pattern area and other areas. It is because the Luminance of the fixed pattern area becomes lower than the other areas due to the degradation of the phosphor, but this phenomenon is not a failure.
On the other hand, when the display pattern is changed, the illuminated areas may maintain their Luminance temporarily (for few minutes). This phenomenon is a characteristic from color S50HW-XD03 itself due to the activation of the discharge surface in the S50HW-XD03 panel, which is normal. If you have an intention of displaying the fixed pattern, the screen-saver technique should be applied to your systems in order to minimize the image retention.

(8) The S50HW-XD03 Module is not intended for the equipments that require extremely high reliability such as aerospace equipments, nuclear control systems or medical equipments for life support.

(9) Based on the requirements of the safety standard (UL, EN etc.), be sure to add the filter that come up to the impact test to the glass pate.

□ ***Notice to the operation and handling of the*** S50HW-XD03 ***Module***.

(1) To prevent defect or failure, please check the cable connections and power-supply condition before power-on.

(2) The S50HW-XD03 Module is controlled by high voltage. Not only during operation but also immediately after power-off, do not disconnect or reconnect the S50HW-XD03 Module's connector because it may result in failure. If you need to disconnect or reconnect, you have to wait at least one minute after power-off.

(3) The S50HW-XD03 Module is equipped with various protection circuits that automatically stop the Module operation, if an interface signal or the power voltage becomes abnormal during operation. If the S50HW-XD03 Module stops suddenly during operation, please check the conditions of input signal or power source before restarting.

(4) For the protection of the circuit, if an abnormal situation is occurred, the high output voltage will be shut down by (watching) the internal input voltage (Vs/ Va/ Vcc). In this case, the Module power resetting is necessary to recover.
There are also fuses in the Vs and Va power supply system to prevent smoking and firing by the excessive current. The protecting function of the address driver of keeping a supervisory device for the internal current is provided in the Va power supply system. Therefore, the number of sub-frames decreases to a proper value when the Ia current exceeds a constant value occasionally.

(5) If an abnormal situation such as disconnecting of the input connector occurs, this Module will be on stand-by, which the supply of high output voltage is stopped even if an external power is being supplied. If a normal signal is inputted after this, normal operation state, operations can be restarted again by re-inputting a normal signal. However, it is necessary to rest the Module power when tVH and/or tHV are less than the minimum value provided in the specification

(6) To ensure reliable operation of the S50HW-XD03 Module and to protect it from overheating, do not wrap or cover it with a cloth or like a sheet during power-on period. Also, do not place the S50HW-XD03 Module in a confined space or any other places of poor ventilation.

(7) If you continue to watch the naked S50HW-XD03 screen(without filter glass) for a long time, your eyes could be fatigued. We recommend you rest your eyes occasionally.

(8) The S50HW-XD03 screen is controlled with the display-data signals and synchronized signals. If noise interferes with those signals, the S50HW-XD03 screen could become unstable and, in some case, would cause a failure. Do not place any equipment that generates excessive EMI/RFI noise near the interface cable of the S50HW-XD03 Module, and keep the cables as short as possible.

(9) Be careful not to break the glass panel when you handle the S50HW-XD03 Module. Also, when handling the S50HW-XD03 Module, you must wear gloves or other hand protection to

prevent injuries that can occur in case when the glass panel is broken.

(10) The glass panel section and drive circuit section of the S50HW-XD03 Module are closely connected and they function as a pair. If the Module is arbitrarily recombined, restructured, or disassembled, SDI will not be responsible for the function, quality, or operational integrity of the modified Module. Do not recombine, restructure, or disassemble it.
(only, the Module for A/S is allowed to be recombined, restructured, or disassembled.)

(11) To avoid a possible electric shock, you must make sure that the power supply voltage of S50HW-XD03 Module is turned off before cleaning. To clean the S50HW-XD03's glass panel, apply water or a natural detergent to a piece of soft cloth or gauze, and wring the cloth tightly before wiping the screen. Make sure that no water comes in contact with the connecting terminals on the side of the glass panel. Do not use chemical solvents, such as paint thinner or benzene, to clean the glass panel.

(12) The drive circuit section of S50HW-XD03 Module uses C-MOS integrated circuits that must be protected from static electricity. Therefore when transporting or delivering the Module, be sure to put the Module in an antistatic bag. When handling the S50HW-XD03 Module, take adequate grounding precautions to prevent static electricity.

(13) When delivering or transporting the S50HW-XD03 Module, you must take special precautions because excessive vibration or shock should not be applied to it. If the Module is dropped, or (if) excessive vibration/shock is applied, the glass panel of the S50HW-XD03 Module may be broken and the drive circuit may be damaged. The packing for delivering or transporting should be made with strict instructions.

(14) When storing the S50HW-XD03 Module, you must select an environmentally controlled place. Avoid any environment in which the temperature or humidity exceeds the specification values. If you are storing it for a long period of time, We recommend that you place the Module together with a dehumidifying agent, such as silica gel, in a moisture-proof bag and keep it in an environmentally controlled place.

(15) The S50HW-XD03 Module is composed of various kinds of materials such as glass plate, metals and plastics. A qualified service technician is required for the disposal of the S50HW-XD03 Module.

□ *Notice of the S50HW-XD03 Module performance*

The S50HW-XD03 Module is the newest display device utilizing the gas discharge technology and digital signal processing technology, and its performances are mostly similar to those of CRT. However, some display performances of the S50AX -****Module are different from the CRT's. Please consider the following notices when you watch the S50HW-XD03 screen.

(1) There is (a) slight Neon luminance shown outside of the effective display area on the glass panel. Conceal this part so that it may not be seen on the display surface.

(2) Depending on the type and time of usage, there may be a slight change in the Luminance and

color. There may be an increase of both X-value and Y-value by 0.05 at the maximum in chromaticity. In this case, adjust it using the external data signal.

(3) Because the S50HW-XD03 Module uses phosphor to emit a light, the phosphor, like a CRT, will be deteriorated in proportion to the display signal and Luminance settings. If the same pattern is displayed continuously (fixed display) for an extended period of time, the Luminance of that area will be decreased over non-lit areas due to the fact that the discharge surface will be more activated comparing to the other areas.

(4) When the Vsync signal timing becomes shorter right after the changing of Vsync frequency (e.g. from 50㎐ to 60H / from 60㎐ to 70㎐) depending on the Multi-Vsync function, an initial Vsync signal of the changed frequency will be disregarded and the S50HW-XD03 screen will be interrupted for 1 frame period in maximum.

(5) Because the S50HW-XD03 Module is a digital processing display device, this Module is equipped with the Error diffusion technology and a Duplicated Sub-Frame method to display the grayscale and false contour improvement. However, you may sometimes find a color false contour, especially in human facial contour, in moving picture due to the difference of display performance comparing to the TV-tube.

(6) If the S50HW-XD03 Module displays some video test patterns that are mostly used in a laboratory or inspection process of the manufacturing facilities, you may find the following subjects. But these subjects sould not be recognized in the failure or defects because the display performance of the S50HW-XD03 Module is equipped with Error diffusion technology and Duplicated Sub-Frame method(for PAL) based on digital processing technique.

<a> Linearity in the grayscale test pattern

If the S50AX -****Module displays the grayscale test pattern (e.g. white color Luminance is gradually changed horizontally or vertically) in a screen, you may find the disparity of Luminance at adjacent grayscale patterns. This behavior is caused by duplicated sub-frame condition(for PAL), display load correction and electrode dependency.

<b> Color contouring and dithering at the stationary picture

If the stationary picture such as a human face or the like is shown in the S50HW-XD03 screen, you may feel some unstable noise at the contour area. This behavior is called the color contouring or dithering, and is caused by the error diffusion condition, display load correction and electroad dependency.

(7) If the S50HW-XD03 Module is operated under inadequate conditions or harsh environment, the screen may become unstable or noisy. This instability is mostly related to ambient temperature, air pressure, input signal instability (include signal noise), input power voltage and strong magnetic field such as MRI/NMR application or superconducting magnet application. Please do not apply the S50HW-XD03 Module to inadequate conditions or harsh environment mentioned above.

Disclaimer

This Specification stipulates the final and comprehensive requirements for the respective products hereof. Beyond this Specification, it is the responsiblity of the customer to explicitly disclose any additional requirements, information or reservations regarding these requirements to Samsung SDI prior to implementation, where any and all disclosures of the customer shall be with an authorized representative of Samsung SDI in writing. Samsung SDI shall not be responsible for safety, performance, functionality or compatability of the system with which the Samsung SDI-supplied components are intergrated unless such features have been expressly communicated and described in the Specification. SAMSUNG SDI MAKES NO GUARANTY OR WARRANTY, EXPRESS OR IMPLIED, INCLUDING BUT NOT LIMITED TO MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, TO ANY PARTY. Moreover, any party should do their own due diligence regarding these requirements prior to implementation.